

Research Team

(603) 7890 8888

research_dept@apexsecurities.com.my

Recommendation:	BUY
Current Price:	RM2.97
Previous Target Price:	N/A
Target Price:	RM4.67
Capital Upside/Downside:	57.2%
Dividend Yield (%):	0.0%
Total Upside/Downside	57.2%

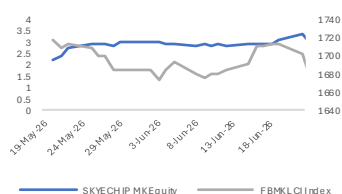
Stock information

Board	MAIN
Sector	Technology
Bursa / Bloomberg Code	5357 / SKYECHIP MK
Syariah Compliant	Yes
ESG Rating	★★★
Shares issued (m)	1,796.0
Market Cap (RM' m)	5,334.1
52-Week Price Range (RM)	3.8-2.01
Beta (x)	N/A
Free float (%)	36.2
3M Average Volume (m)	n/a
3M Average Value (RM' m)	n/a

Top 3 Shareholders

	(%)
Teh Chee Hak	27.9
Fong Swee Kiang	27.8
Skc Team 2 Sdn Bhd	7.9

Share Price Performance



	1M	3M	12M
Absolute (%)	10.0	N/A	N/A
Relative (%)	11.7	N/A	N/A

Earnings summary

FYE (Dec)	FY27F	FY28F	FY29F
Revenue (RM'm)	212.9	276.0	344.9
PATAMI (RM'm)	90.2	123.6	154.9
CNP (RM'm)	93.2	127.4	159.6
EPS - core (sen)	5.2	7.1	8.9
P/E(x)	58.2	42.6	34.0

Source: Company, Apex Securities

SkyeChip Berhad

ASEAN's only pure-play semiconductor IP bet

- SKYECHIP is the only profitable, pure-play semiconductor IP company listed across ASEAN, designing and licensing silicon-proven memory interface IP (HBM3/HBM3E, DDR5, LPDDR5), NoC IP, and UCIe D2D interface IP to AI chip designers globally, alongside custom ASIC design services for IoT and AI inference.
- We project FY26-FY29F core earnings to grow at a c.48% CAGR, driven by the ramp of HBM3E/HBM4 IP licensing across Chinese, American, and Korean AI chip customers, geographic diversification (US revenue surging from 5.7% to 23.1% of Group in FY26 with South Korea entering as a new market), and operating leverage as gross margin expands from 45.1% to 50.9% in FY29F on the IP licensing flywheel.
- We initiate coverage with a BUY rating and a TP of RM4.67, based on 76.6x mid-FY28F Core EPS of 6.1 sen (a 15% premium to the 66.1x peer average FY27 forward P/E). We like SKYECHIP for its: (i) scalable IP licensing model with near-zero marginal cost per additional licence, (ii) silicon-proven HBM3E credentials at 4nm that only a handful of companies globally can match, and (iii) ASEAN scarcity premium with limited comparable listed peers across the region.

Key Investment Highlights

Only commercialised HBM3/HBM3E IP house in ASEAN. SKYECHIP achieved first-time silicon success for its HBM3E interface IP at 8,800 Mbps on Samsung SF4X (4nm), making it one of very few companies globally with commercially deployed HBM3E memory interface IP at an advanced process node. In a market where customers will not risk unproven interfaces on chips costing **USD50-100m** to tape out, silicon-proven status is the defining and hardest-to-replicate moat. The IP portfolio spans the full memory interface stack (DDR5, LPDDR5, HBM3, HBM3E, with HBM4 and LPDDR6 in development), NoC IP with the proprietary RAPTuner EDA tool, and UCIe-compliant D2D interface IP, giving customers single-vendor coverage that reduces integration risk and increases switching costs. The HBM IP market is projected to grow from USD201m (2024) to USD513m (2032) at a **12.4% CAGR**, and every successive generation of AI chip uses more HBM with higher bandwidth, with NVIDIA's roadmap alone representing a 6.4x increase in HBM per chip from H100 to Rubin Ultra.

Scalable IP licensing flywheel with accelerating operating leverage. The business model is fundamentally different from most semiconductor companies: SKYECHIP creates design blueprints for memory interfaces and on-chip interconnects and licenses these designs to customers who integrate them into their own chips. Once the IP is silicon-proven, each subsequent licence generates revenue with near-zero marginal cost. This flywheel is now demonstrably turning as revenue per engineer has grown from RM347k (FY24) to RM425k (FY26), and we forecast it reaching RM690k+ by FY31F as the licensable portfolio broadens and each IP block is licensed to progressively more customers. Gross margin expanded from 42.2% (FY25) to **45.1% (FY26)**, with Q4 FY26 printing **64.0%** in an IP-heavy quarter, and we forecast continued expansion toward **54.7% by FY31F**. FY26 results confirmed the trajectory: revenue RM155.0m (+29.7% YoY), PAT RM48.5m (+35.0% YoY), customer base nearly doubling from 14 to 26, and US revenue surging to 23.1% of Group revenue from 5.7% in FPE Oct 2025.

Geographic diversification validates IP quality beyond China. The most significant development in FY26 was the emergence of the US as **23.1%** of Group revenue (RM35.8m) and South Korea as a new market at 1.0% (RM1.5m), reducing China/Taiwan concentration from 90.6% (FPE Oct 2025) to 73.8% in FY26. This is not merely a diversification story but a product quality certification: US AI chip startups are sophisticated, well-funded buyers with access to all global IP providers including Synopsys, Cadence, and Rambus at full scale, and the fact that they are choosing SkyeChip's interface IP without any geopolitical pressure to do so is the strongest possible independent validation of its technical credibility. Q4FY26 alone saw US revenue of RM28.9m (49% of Q4 revenue), a single-quarter US run-rate that annualises to

RM115m+. South Korea's entry via the Samsung Foundry CONNECT listing (February 2026) opens the K-Nvidia ecosystem where Rebellions (USD850m funded, KOSPI IPO targeting Q3 2026) and FuriosaAI (KRW3 trillion valuation) are building chips using HBM3E and UCIe, both directly within SkyeChip's IP portfolio.

Unpriced optionality from Arm CSS and Samsung Foundry CONNECT. On 23 June 2026, SkyeChip signed the definitive agreement for access to the Arm Flexible Access (AFA) platform with MIDA, granting full access to Arm's chip design platform for product experimentation and development without upfront licensing fees. The Arm Compute Subsystem (CSS) platform, for which conditional approval was received on 14 April 2026, remains under evaluation, with RM82.0m of IPO proceeds ring-fenced for CSS-based development. We have not included any AFA or CSS revenue in our base case forecasts, but the incremental opportunity could reach **RM14-21m** per annum from FY28-FY29F onwards if 2-3 Arm-based contracts are secured, representing **5-8%** upside to our FY28F revenue estimate. Separately, SkyeChip's UCIe-AP 32G PHY IP was listed on Samsung Foundry CONNECT in February 2026, enabling every Samsung Foundry customer globally to discover and engage with SkyeChip at zero incremental cost, a channel that appears to have generated its first Korean customer engagement shortly after going live.

We initiate coverage on SKYECHIP with a BUY rating and a target price of RM4.67, based on 76.6x mid-FY28F Core EPS of 6.1 sen (a 15% premium to the 66.1x peer average FY27 forward P/E). We like SKYECHIP for its: (i) scalable IP licensing model with a FY26-FY29F core earnings CAGR of c.48%, (ii) silicon-proven HBM3E credentials at 4nm and the broadest memory IP portfolio in its size class, (iii) ASEAN scarcity premium as the only profitable pure-play semiconductor IP company listed on Bursa Malaysia, and (iv) a valuation of 57.2x FY27 P/E and 41.9x FY28 P/E at the current price of RM2.97, a **14% and 5% discount to the peer simple averages** of 66.1x and 44.2x respectively despite offering materially superior growth, which caps downside risk while offering substantial scope for re-rating as SkyeChip continues to demonstrate its ability to win customers on merit in the US and Korea, de-risk its China geographic concentration, and unlock new growth levers from Arm CSS and next-generation IP (HBM4, LPDDR6, automotive NoC). Our **76.6x** target multiple sits below Arm (162.0x FY27) and GUC (104.1x), but above M31 (66.3x), Faraday (55.8x), and Rambus (43.4x), reflecting SkyeChip's superior growth profile and ASEAN scarcity premium while acknowledging the China concentration risk (62.6% of FY26 revenue), Pioneer Status renewal uncertainty, and the early-stage listed track record that will be de-risked through execution over time.

Earnings Summary

FYE Mar (RM m)	FY25	FY26	FY27F	FY28F	FY29F
Revenue	119.5	155.0	212.9	276.0	344.9
EBITDA	43.4	60.5	107.7	150.1	196.4
Pre-tax profit	37.0	50.0	94.0	129.4	161.4
Net profit	36.0	48.2	90.2	123.6	154.9
Core net profit	37.1	49.7	93.2	127.4	159.6
Core EPS (sen)	2.1	2.8	5.2	7.1	8.9
P/E (x)	146.1	109.1	58.2	42.6	34.0
P/B (x)	42.9	27.7	8.7	7.3	6.0
EV/EBITDA (x)	124.2	88.4	46.3	32.7	24.4
Dividend Yield (%)	0.0%	0.0%	0.0%	0.0%	0.0%
Net Gearing (%)	NET CASH	NET CASH	NET CASH	NET CASH	NET CASH

Source: Company, Apex Securities

Investment Thesis and Drivers

Thesis 1: Only Commercialised HBM3/HBM3E IP House in Asean

What is HBM? High Bandwidth Memory (HBM) is an advanced memory technology that vertically stacks multiple DRAM dies and connects them using through-silicon vias (TSVs), delivering dramatically higher data transfer speeds than conventional memory. While a high speed DDR5 module delivers roughly 50 GB/s of bandwidth (Kingston Technology), a single HBM3E stack can deliver up to 1,200 GB/s (Siemens) implying a **c.24x** improvement. As a result, HBM has become the de facto memory standard for AI accelerators because training and running large language models demands enormous memory bandwidth that traditional architectures simply cannot provide or replicate.

However, an HBM stack is useless without a memory interface to connect it to the processor. The memory interface: comprising a physical layer (PHY) and a digital controller is the "highway" that manages data flow between the processor die and the HBM stacks sitting beside it on the interposer. This interface must operate at extraordinary speeds with near-zero error rates, requiring deep expertise in high-speed analogue/mixed-signal design, signal integrity, and power management. **This is precisely what SKYECHIP designs and licenses.**

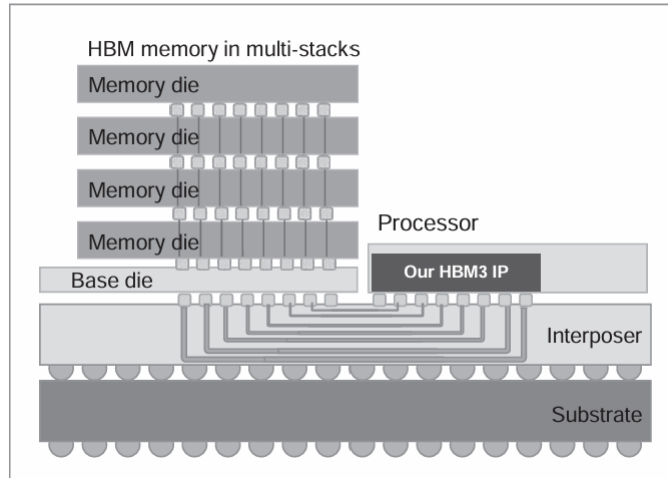
SKYECHIP is the only company in Malaysia, and one of very few globally with commercially deployed HBM3 and HBM3E interface IP up to the 4nm process node. The Group's IP portfolio spans the full memory interface stack: DDR5, LPDDR5, HBM3, and HBM3E + controller IP, alongside Network-on-Chip (NoC) IP for on-chip data routing. This breadth of coverage across both memory standards and process nodes gives SKYECHIP a significant competitive advantage, as customers can source multiple IP blocks from a single proven vendor rather than managing integration risk across multiple suppliers.

The competitive moat in memory interface IP is substantial. Designing an HBM interface requires years of accumulated know-how in high-speed analogue circuit design, combined with access to advanced foundry process development kits (PDKs) and extensive silicon validation. An IP block is only commercially valuable once it has been "silicon-proven" - meaning it has been fabricated on a real chip, tested at production speeds, and demonstrated to work reliably. Customers will not risk an unproven interface on a chip that may cost up to **c.USD50-100m** (Patent PC) to tape out at 4nm. SKYECHIP's silicon-proven status at 4nm creates a powerful lock-in: once a customer designs a chip around SKYECHIP's HBM3E, switching to a competitor's interface for the next generation would require a costly and risky redesign cycle.

The HBM market is experiencing explosive growth. According to Precedence Research, the global HBM device market was valued at USD7.27bn in 2025 and is projected to grow at a CAGR of c.25% through 2035, driven by insatiable demand from AI accelerators. Within this, the HBM IP market (comprising controller IP and PHY IP specifically for HBM interfaces) was valued at USD201m in 2024 and is projected to reach USD513m by 2032 at a 12.4% CAGR (SNS Insider), representing SkyeChip's directly addressable segment. SK Hynix, the global HBM device market leader with **c.62%** share (CounterPoint), has confirmed that its HBM capacity is sold out through 2026 and has forecast 30% annual HBM growth through 2030. In February 2026, Samsung commenced initial shipments of sixth-generation HBM4, while in March 2026, Samsung and AMD signed an MOU to expand strategic collaboration on HBM4 supply for AMD's Instinct MI455X GPUs, signalling confidence in long-term HBM growth. The HBM supply chain is operating at full tilt, and every HBM stack shipped requires a memory interface, the IP that SKYECHIP provides..

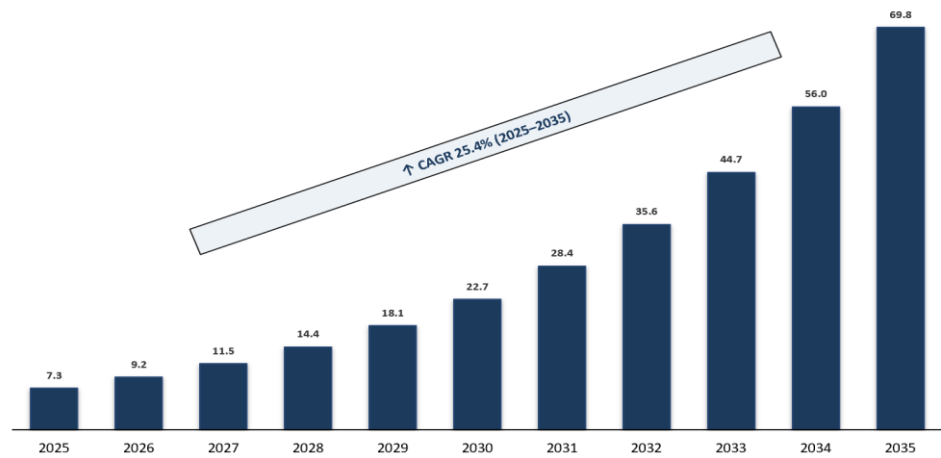
The trajectory is clear: each successive generation of AI chip uses more HBM with higher bandwidth, driving demand for ever-more-sophisticated memory interface IP. NVIDIA's roadmap alone from 80 GB per H100 to 288 GB per Blackwell Ultra to 512 GB per Rubin Ultra represents a projected **c.6.4x** increase in HBM per chip, and each of these chips needs a SKYECHIP-class interface. **Hence, we believe SKYECHIP is exceptionally well positioned to capture a meaningful share of this structural growth as one of the few proven HBM interface IP providers globally.**

Figure 1: HBM Interface IP Graphic



Source: Company

Figure 2: Global HBM Market Size Projections



Source: Precedence Research, Apex Securities

Figure 3: HBM Consumption by Major AI Chip Platforms

Platform	Company	HBM Gen	Stacks	Total HBM	Bandwidth
H100 SXM5	NVIDIA	HBM3	5	80 GB	3.35 TB/s
H200 SXM	NVIDIA	HBM3E	6	141 GB	4.8 TB/s
Blackwell Ultra GB300	NVIDIA	HBM3E	8	288 GB	8.0 TB/s
Rubin Ultra	NVIDIA	HBM4	—	~512 GB	TBD
MI300X	AMD	HBM3	8	192 GB	5.3 TB/s
MI455X	AMD	HBM4	—	TBD	TBD
TPU v5p	Google	HBM	—	95 GB	2.8 TB/s

Source: Nvidia, AMD, Samsung, Google, Apex Securities

Figure 4: Memory Interface IP Portfolio

IP Product	Description	Key Specification	Max Data Rate	Max Bandwidth	Status
HBM3 PHY + Controller	High-bandwidth memory for AI / HPC data centres	1024-bit interface; DFI 5.1; supports 2.5D/3D packaging; controller + PHY + I/O	6.4 Gb/s (6,400 MT/s)	819 GB/s per stack	Commercialised (2022)
HBM3E PHY + Controller	Enhanced HBM for next-gen AI chips; silicon first-time success at 4nm / 8,800 Mbps	1024-bit interface; DFI 5.1; two tapeouts confirmed; up to 9,600 MT/s	≥8.0 Gb/s (9,600 MT/s)	≥1,024 GB/s per stack	Commercialised (2024)
DDR5 PHY + Controller	Standard DRAM interface for servers and PCs	DFI 5.0 compliant; one-stop PHY & Controller; avg random efficiency >85%; upgradable to 6,400 MT/s	Up to 6,400 MT/s	Up to 51.2 GB/s	Commercialised
LPDDR5 / LPDDR5x PHY + Controller	Low-power DRAM for mobile, edge and AI applications	Conforms to JESD209-5C; DFI 5.1; avg random efficiency >85%; DFE/FFE equalization; LPDDR5x up to 10,667 MT/s	≥8,533 MT/s (LPDDR5x)	≥68.3 GB/s	Commercialised (enhanced Jul 2025)
LPDDR4 / LPDDR4x PHY + Controller	Low-power DRAM for mobile and IoT devices	Conforms to LPDDR4/4x JEDEC standard; memory controller + PHY	Up to 4,267 MT/s	Up to 34.1 GB/s	Commercialised (2022)
Future Development: R&D Stage (target specifications; not yet commercialised)					
LPDDR6 PHY + Controller	Next-generation low-power DRAM (in development)	Target: 14.4 Gb/s max data rate; 96-bit bus; 172.8 GB/s bandwidth; -2-3 pJ/bit energy efficiency	14.4 Gb/s (target)	172.8 GB/s (target)	R&D Stage
HBM4 PHY + Controller	Next-generation HBM for future AI accelerators (in development)	Target: ≥8 Gb/s per pin; 2,048-bit interface; ≥2,048 GB/s bandwidth; -0.4-0.5 pJ/bit energy efficiency	≥8.0 Gb/s (target)	≥2,048 GB/s (target)	R&D Stage

Source: Company, Apex Securities

Thesis 2: Scalable IP Licensing Model : The “Software Royalty” of Semicon

SKYECHIP's business model is fundamentally different from most semiconductor companies. The Group does not manufacture any physical product. Instead, it creates IP, the design blueprints for memory interfaces and on-chip interconnects and licenses these designs to customers who integrate them into their own chips. This is analogous to a software licensing model wrapped inside a semiconductor shell: once the IP is designed and silicon-proven, each subsequent license generates revenue with minimal incremental cost.

The business comprises three revenue streams with distinct economics:

Standard Silicon IP is the high-margin core (silicon IP comprised 77.0% or RM119.4m of FY26 revenue, up 39.3% from RM85.7m in FY25). These are pre-designed, reusable building blocks that have been silicon-proven and can be licensed to multiple customers without modification. A customer designing an AI chip that needs an HBM3E interface can license SKYECHIP's proven IP block, integrate it into their chip design, and proceed to tape-out with confidence that the interface will work. The typical licensing structure involves an upfront access fee plus ongoing support and maintenance payments. Based on our segment-level estimates, gross margins on the silicon IP segment are approximately **c.47%**, as the marginal cost of licensing a proven IP block to an additional customer is near-zero, with the engineering work done once during initial development.

Custom Silicon IP involves modifications and customisations of the Group's standard IP blocks to meet specific customer requirements. (Note: The Q4 FY26 quarterly report does not separately break out standard vs custom silicon IP; the combined silicon IP segment contributed 77.0% of FY26 revenue.) This generates higher revenue per engagement but requires dedicated engineering resources.

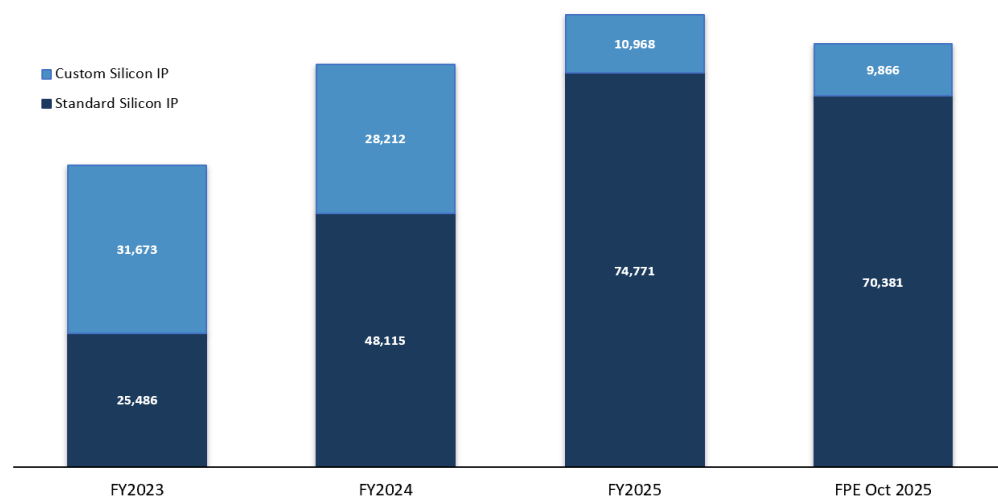
Custom ASIC (22.3% or RM34.6m of FY26 revenue, up from 9.4% in FPE Oct 2025 and 26.7% in FY25) is full-chip design and development of application-specific integrated circuits, primarily for IoT and AI inference applications. This segment was launched in FY24, grew rapidly to **c.26.7%** of FY25 revenue, and then moderated to **c.22.3% of FY26 revenue** of FPE revenue as IP licensing scaled. ASIC design is project-based and more engineering-intensive, with gross margins of **c.42%**. However, ASIC serves a critical strategic purpose: it creates deep customer relationships. Customers who commission a custom ASIC typically become IP licensing customers for subsequent chip generations, as they integrate SKYECHIP's proven IP blocks into future designs. In this way, ASIC functions as a customer acquisition channel that feeds the higher-margin IP licensing core.

The parallels to Arm Holdings and Rambus are instructive. Arm licenses its CPU architecture IP to chip designers worldwide, the design is done once, and Arm collects license fees and royalties from hundreds of customers. Arm trades at c.162.0x FY27 P/E, reflecting its monopolistic position in mobile compute and accelerating AI/data centre penetration. Rambus licenses memory interface IP (specifically, memory controller and PHY designs), a business model closer to SKYECHIP's, albeit at larger scale and with a broader product portfolio. Rambus trades at c.43.4x FY27 P/E. SKYECHIP operates in the same fundamental model: design once, license many, collect near-pure profit on incremental licenses. At 57.2x FY27 P/E and 41.9x FY28 P/E at the current price of RM2.97, SKYECHIP trades at a premium to Rambus (43.4x FY27) but at a substantial discount to Arm (162.0x FY27), despite offering a materially faster growth rate (FY27-28F EPS growth of 36.6% and FY26-29F core earnings CAGR of c.48% vs Rambus at 23.8% and Arm at 38.0%), suggesting the market has narrowed but not yet fully closed the valuation gap warranted by the IP licensing flywheel and ASEAN scarcity premium.

The IP licensing flywheel creates a compounding dynamic. Each new IP block that SKYECHIP develops and silicon-proves adds to its licensable portfolio. SkyeChip has allocated RM56.4 million over 36 months from IPO proceeds for the development of its next-generation IP portfolio, covering new memory interface IP (HBM4, LPDDR6), Network-on-Chip IP, and automotive IP. While individual IP licensing contracts are structured on a per-project basis, SkyeChip's standard silicon IP has generated recurring revenue since its commercial launch in 2022 across multiple customers and geographies. As each new chip design cycle or process node upgrade typically requires a fresh licensing engagement, the cumulative revenue potential from a single IP block across multiple customers and generations extends well beyond the initial contract term and as the portfolio grows, revenue can scale without proportional increases in headcount. **This is the fundamental driver of operating leverage in IP licensing businesses, and it explains why established IP companies like Arm and Rambus sustain premium valuations.**

Revenue growth has been exceptional. Revenue grew from **RM57.2m** in FY23 to **RM77.1m** in FY24 and **RM119.5m** in FY25, a two-year CAGR of **44.5%**. The full-year FY26 results (year ended 31 March 2026) confirmed this momentum, with the Group delivering RM155.0m in revenue (up 29.7% YoY from RM119.5m in FY25), with PAT of RM48.5m (up 35.0% YoY) and an improved gross margin of 45.1% (vs 42.2% in FY25). Notably, Q4 FY26 alone contributed RM58.9m in revenue and RM31.5m in PAT, demonstrating accelerating momentum. The FY26 customer base expanded to 26 customers, up from 14 in FY25, while US revenue emerged as 23.1% of Group revenue (RM35.8m), significantly diversifying the geographic mix. This exceptional growth trajectory reflects the expansion of the IP portfolio, the near doubling of the customer base, and the successful penetration of the US market.

Figure 5: Silicon IP Segment Revenue



Source: Company, Apex Securities

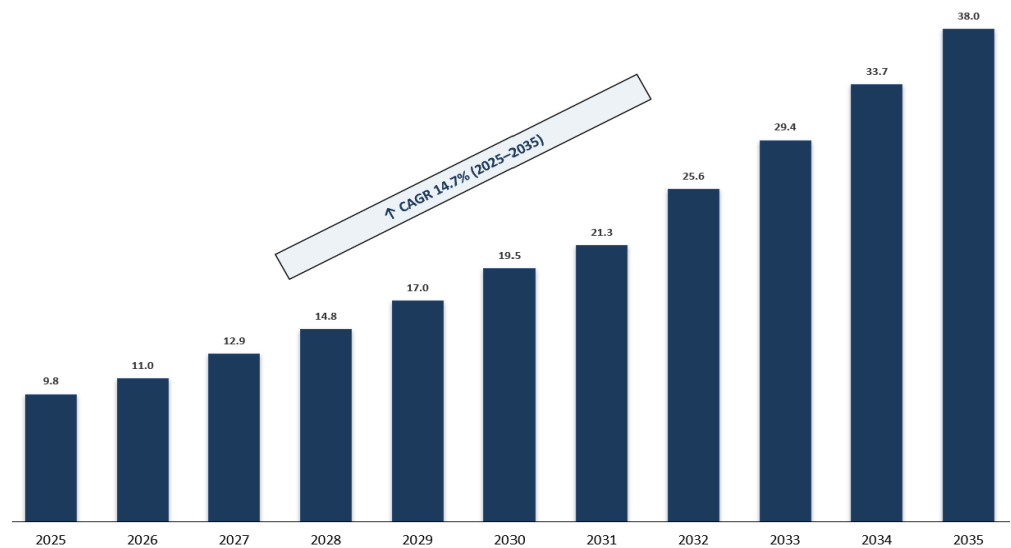
Thesis 3: Riding the AI Chip Supercycle: TAM Expansion Across HPC/Memory

The AI infrastructure buildout is the largest capital expenditure programme in technology history, and SKYECHIP is positioned to benefit from every dollar spent. In 2026, the four largest hyperscalers: Amazon, Google, Meta, and Microsoft, have collectively committed to spending **c.US\$750bn** on capital expenditure, nearly doubling the record **c.USD410bn** spent in 2025. Including Oracle, total Big Five hyperscaler capex is approaching **c.USD775bn**. The vast majority of this spending is estimated at **c.75% or USD450-500bn+** is directed at AI infrastructure: GPUs, custom AI accelerators, servers, networking, and data centres (Creditsights).

Every AI chip at the heart of these data centres requires memory interfaces and on-chip interconnects. A single NVIDIA Blackwell Ultra GPU uses up to 288 GB of HBM3E, with each HBM stack connected to the processor through an interface that must be designed, verified, and silicon-proven. Custom AI accelerators being developed by the hyperscalers themselves, Amazon's Trainium, Google's TPU, Microsoft's Maia all face the same requirement. And every one of these interfaces represents a potential licensing opportunity for companies like SKYECHIP.

The semiconductor IP market is growing in lockstep. According to Global Market Insights, the semiconductor IP market was valued at **c.USD9.8bn** in 2025 and is estimated to grow at a CAGR of **c.14.7%** through 2035, reaching **c.USD38bn**. Within this, memory IP is the fastest-growing sub-segment, driven by the proliferation of HBM and advanced DDR standards. Interface IP, which includes memory interfaces and high-speed serial links, is the fastest-growing IP category by revenue. SKYECHIP operates squarely at the intersection of the two fastest-growing segments: memory interface IP and AI-related custom ASIC design.

Figure 6: Global Semiconductor IP Market Size Projections



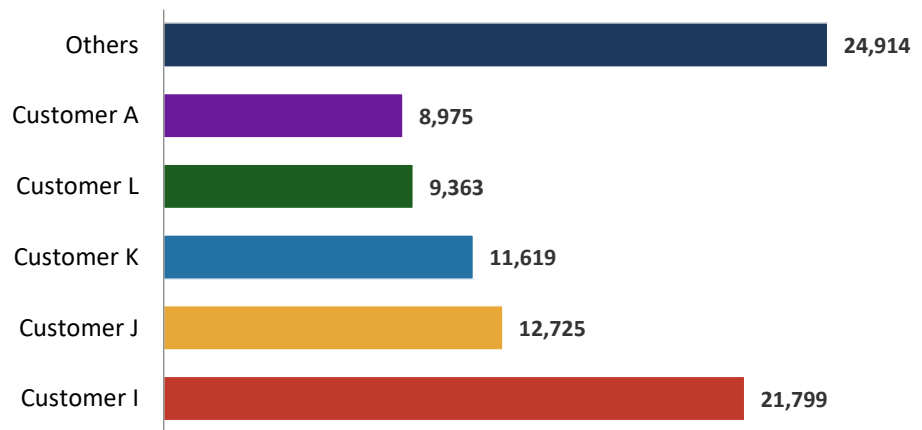
Network-on-Chip (NoC) the second growth pillar. As chip designs become more complex integrating dozens of CPU cores, GPU clusters, AI accelerators, and multiple I/O interfaces onto a single die, the on-chip communication fabric becomes a critical bottleneck. **NoC IP provides a structured, scalable interconnect that efficiently routes data between these components.** The NoC market is smaller than memory interface IP but is growing rapidly as chiplet-based architectures gain traction. Chiplet-based architectures are now being adopted across virtually all large compute and networking chips in development, driven by yield optimisation at advanced nodes, reduced design costs, and the need for heterogeneous integration. According to Alphawave Semi, the key to successful chiplet-based designs is low-latency, low-power interconnect between functional blocks: precisely the role played by SkyeChip's NoC IP with UCle die-to-die interconnection standards proving crucial to the ecosystem. SkyeChip's NoC IP

complements its memory interface portfolio, allowing the Group to offer customers a more complete set of IP building blocks across both memory and interconnect.

The Chinese AI chip ecosystem is a particularly strong demand driver for SKYECHIP. US export controls have progressively restricted Chinese companies' access to the most advanced AI chips and semiconductor manufacturing equipment. This has forced Chinese AI chip designers to develop indigenous alternatives, creating massive demand for third-party IP blocks from non-US suppliers. **SKYECHIP, as a Malaysian company, is not subject to US export controls (its IP is not on restricted lists), making it an attractive partner for Chinese chip designers who need proven memory interface IP but cannot or prefer not to source from US companies like Synopsys or Cadence.**

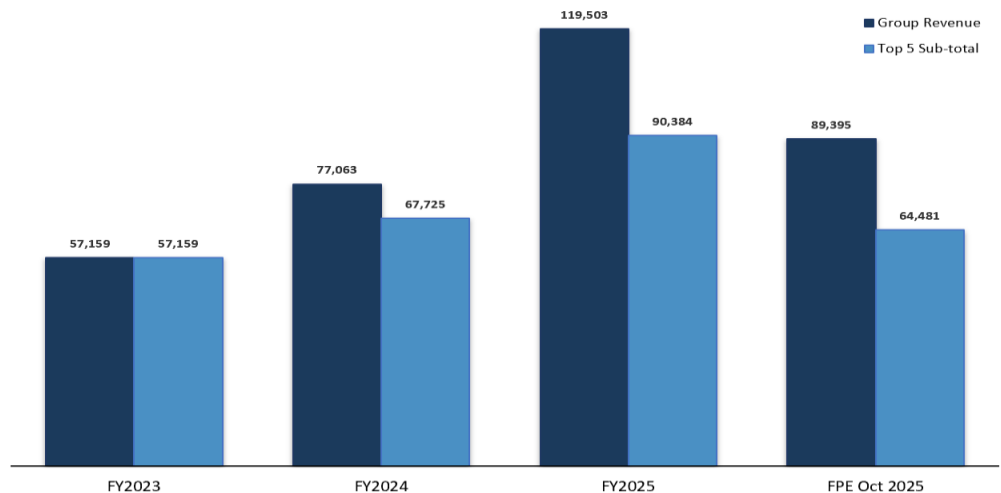
SkyeChip's top five customers by FPE Oct25 revenue are all private Chinese IC design companies based in cities including Shanghai, Guangzhou, Hefei, and Shenzhen, collectively representing the majority of the group's China revenue. China and Taiwan together accounted for **73.8% of FY26 revenue (China: 62.6%, Taiwan: 11.2%), a meaningful improvement from 90.6% (China: 73.3%, Taiwan: 17.3%) in FPE Oct 2025, driven by the emergence of the US as 23.1% of FY26 revenue**, reflecting concentrated but high-growth demand from the Chinese AI and HPC semiconductor ecosystem

Figure 7: FPE OCT2025 Customer Revenue Breakdowns



Source: Company, Apex Securities

Figure 8: Group Revenue vs Top 5 Customers



Source: Company, Apex Securities

Figure 9: Why Chinese AI Chip Designers need Skyechip

Factor	Implication for SkyeChip	SkyeChip Advantage
US export controls on AI chips	Chinese firms must design their own AI accelerators	Direct demand driver for SkyeChip's HBM interface IP
US export controls on EDA tools	Creates preference for non-US IP suppliers	Malaysian domicile gives SkyeChip geopolitical neutrality
HBM3E interfaces required for competitive AI chips	SkyeChip provides proven, silicon-ready IP	Only ASEAN company with commercialised HBM3E IP
Limited alternative suppliers	Few non-US companies offer HBM interface IP at advanced nodes	One of only ~8 HBM IP providers globally
IP licensing not currently restricted	SkyeChip's Malaysian domicile is a key advantage	IP licensing sits outside current US export control frameworks

Source: Company, Apex Securities

Thesis 4: Deep Technical Moat: 113 Patents, 300+ IC Designers.

SKYECHIP's competitive moat is built on three pillars: intellectual property, human capital, and silicon-proven track record.

Pillar 1: Intellectual property. The Group holds 36 registered patents and 77 pending patent applications across Malaysia, China, and the USA, for a total portfolio of 113 patents. Beyond formal patents, SkyeChip's team of 365 technical professionals possesses accumulated know-how in silicon IP design at advanced process nodes, developed through continuous R&D and validated by repeated silicon tapeouts. The Group also continuously develops in-house design methodology improvements to further enhance its technical capabilities.

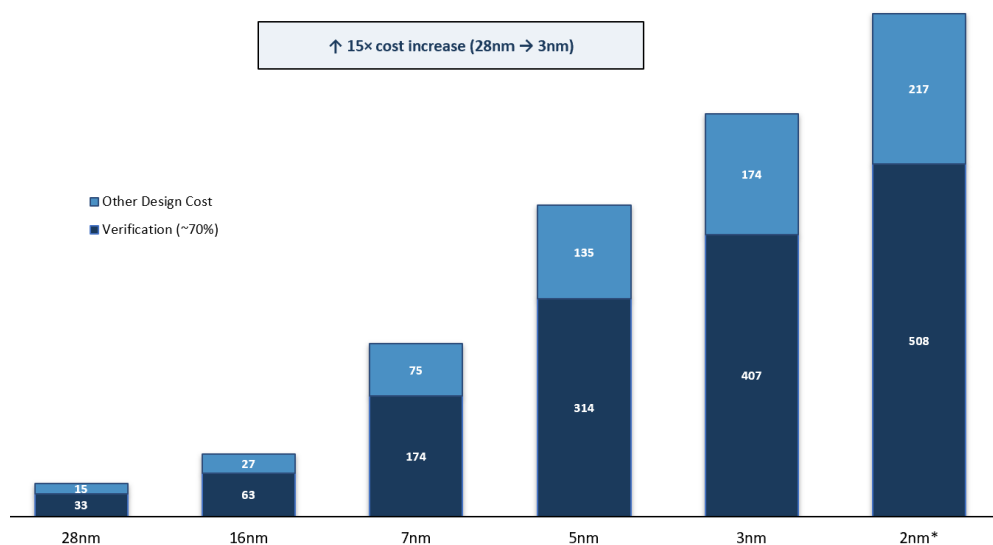
Pillar 2: Human Capital. SkyeChip's technical team comprises 365 professionals as at the LPD, led by CTO Teh Chee Hak who previously served as chief architect at Intel Microelectronics, where he was responsible for the architecture and microarchitecture of FPGA products and IPs across his tenures at Intel Microelectronics and Altera Malaysia from 2000 to 2020. The Group provides structured training programmes requiring each engineer to complete 110 hours of training across 25 modules within their first year, emphasising advanced IC design and verification across digital and analog VLSI methodologies. **High barriers to entry in semiconductor IP: including the depth of engineering expertise required to design silicon-proven memory interface IP at advanced process nodes, underpin the Group's competitive positioning.**

Pillar 3: Silicon-proven track record. In the semiconductor IP market, 'silicon-proven' status: meaning the IP has been fabricated on a real chip, tested under production conditions, and confirmed to work reliably is the gold standard for commercial adoption. SkyeChip has completed two HBM interface IP tapeouts supporting data rates up to 9.6 Gb/s, with HBM3E commercialised in 2024 following a silicon first-time success at 4nm. Replicating this achievement requires access to advanced foundry PDKs, significant mask set and wafer expenditure, and extensive testing and characterisation the prospectus allocates **c.RM56.4 million** for the next generation of silicon IP development alone. The barriers to entry in advanced HBM interface IP is significant given the specialised technical expertise, PDK access, EDA tool availability, and extended development cycles of several years as the primary constraints on new entrants.

The rising cost of chip design reinforces demand for licensed IP. The economics of advanced chip design have become increasingly prohibitive, reinforcing demand for licensed IP. According to IBS, chip design costs have escalated from **c.USD217m at 7nm to c.USD590m at 3nm, reaching USD1.5bn for complex GPU designs**, with 2nm projected to approach **USD725m or more**. Verification alone accounts for over **c.70%** of total development cost (Cadence; Global Semiconductor Alliance), making pre-verified, silicon-proven IP blocks an essential cost-

reduction tool. A customer integrating SkyeChip's HBM3E interface IP avoids designing, taping out, and validating a memory interface from scratch, a process SkyeChip's own prospectus values at **RM56.4 million over 36 months** for a single generation of silicon IP. A chip designer using SKYECHIP's silicon-proven HBM3E interface can avoid months of development time and tens of millions of dollars in design and verification costs. This value proposition becomes more compelling with every process node advance, as the cost of designing from scratch escalates further.

Figure 10: Chip Design Cost by Process Node (USD Mn)



Source: IBS, Marvell, Semiconductor Engineering, Cadence, Apex Securities

R&D intensity signals long-term commitment. RM211.5m or **c.60%** of the RM352m IPO proceeds is allocated to direct R&D, specifically the R&D of IC products (RM155.1m, 44.1%) and R&D of silicon IP (RM56.4m, 16.0%), covering next-generation IP development including HBM4, LPDDR6, RISC-V SoC, new NoC IP, and 2nm process node migration. A further RM74.8m (21.2%) is allocated to R&D-enabling infrastructure computing labs and EDA tools, bringing total technology investment to over **c.80% of gross proceeds**. For context, Arm Holdings the world's leading semiconductor IP licensor invested USD2.0bn+ in R&D in FY2025, representing approximately 50% of its **c.USD4.0bn** revenue. SkyeChip's R&D allocation, while smaller in absolute terms, reflects a comparable investment intensity relative to its proceeds, underscoring the Group's commitment to maintaining its technological edge in an industry where standing still means falling behind.

Access to advanced process nodes. SkyeChip has access to foundry PDKs enabling IC design on advanced process nodes down to 3nm, and in January 2025 joined the Intel Foundry Accelerator IP Alliance, which provides access to Intel Foundry's advanced process technologies, complementing the Group's silicon IP design capabilities. Membership of the Intel Foundry Accelerator IP Alliance also opens a strategic pathway for SkyeChip to develop and qualify IP for Intel's upcoming process nodes, a potentially significant opportunity given Intel Foundry's ambitions to re-establish leadership in advanced semiconductor manufacturing with its 18A and 14A process nodes targeted at AI and HPC customers. The IPO-funded R&D programme explicitly targets development of silicon IP for 2nm process nodes, ensuring the Group's IP portfolio remains relevant across multiple technology generations. As each new process node requires IP to be redesigned and re-validated for the new manufacturing process, node transitions represent natural opportunities for renewed licensing engagements, a structural characteristic of the silicon IP licensing model that underpins recurring revenue potential.

Thesis 5: ASEAN Scarcity Premium - No Comparable Listed Peer

“SKYECHIP is the only profitable, pure-play semiconductor IP company listed on Bursa Malaysia and arguably across all ASEAN exchanges. This scarcity creates a structural valuation premium that we believe the market has yet to fully price in.”

To put this in perspective: there are hundreds of semiconductor companies listed across ASEAN exchanges, but virtually all of them are in packaging/testing (OSAT), assembly, equipment, or contract manufacturing. SKYECHIP occupies a unique position as a pure-play IC design and IP licensing company. One of the only other Malaysian-listed IC design company, Oppstar, is currently loss-making (-RM12.2m in Losses) with a market capitalisation lower than Skyechip, placing it in an entirely different league from SKYECHIP.

The scarcity premium is a well-established phenomenon in capital markets. When Arm Holdings listed on NASDAQ in September 2023 at c.104x P/E, the valuation was widely debated, but the stock subsequently rallied as investors paid up for the only major semiconductor IP company available in public markets. Arm remains one of the only large-cap semiconductor IP play globally, and its premium valuation reflects this scarcity. SKYECHIP, while far smaller, occupies an analogous position within the ASEAN investment universe: it is the only profitable, growth-stage semiconductor IP company available to investors seeking exposure to the AI chip value chain through a listed Malaysian vehicle.

Malaysia's national semiconductor ambitions further enhance SkyChip's strategic positioning. Under the National Semiconductor Strategy (NSS), part of Malaysia's NIMP 2030 framework, IC design has been designated a strategic national priority, with the government's decade-long **USD250m (c.RM1.0bn)** partnership with Arm Holdings targeting the creation of 10 local chip champions collectively generating up to **c.USD20bn** in annual revenue within five to seven years. On 11 May 2026, SkyChip was formally presented with an offer letter granting access to Arm Flexible Access (AFA), making it one of only three Malaysian chip design firms (alongside GreatAsic Technology and Oppstar Technology) to receive formal Arm access tokens under this programme, in a ceremony officiated by the Economy Minister. On 23 June 2026, SkyChip signed the definitive agreement for AFA access with MIDA, formalising the offer and granting full access to Arm's chip design platform for product experimentation and development without upfront licensing fees, making it the second of the three recipients to execute a definitive agreement (after Oppstar on 25 May 2026). SkyChip also received conditional approval for access to the Arm Compute Subsystem (CSS) platform on 14 April 2026, with the definitive agreement still under evaluation given the scale of the undertaking. This positioning within Malaysia's national semiconductor initiative, now reinforced by the execution of the AFA definitive agreement, validates SkyChip's standing as a front-end technology owner and could yield broader policy support, including preferential access to government-linked investment mandates, the pending Pioneer Status renewal, and national semiconductor development programmes.

Figure 11: Chip Design Cost by Process Node (USD Mn)

Metric	SkyeChip	Oppstar
Market Cap (RM m, as at 11 May 2026)	RM 1,581m	RM 561m (up 100+% on since Arm token announcement)
FY25 Revenue (RM m)	RM 119.5m +55% vs FY24	RM 64.0m +12% vs FY24
FY25 PAT (RM m)	RM 35.9m Profitable	RM -12.2m Loss-making (vs +RM15.54m in FY24)
Net Margin (%)	30.0% Consistently profitable since FY23	(-19.0%) Turned loss-making in FY25
Revenue CAGR (2-yr, FY23–FY25)	44.6%	48.6%
Technical Personnel	365 IC designers Architects, analogue, digital & physical design	305 employees Mix of design and service staff
Patents (registered + pending)	113 36 registered + 77 pending (MY, CN, USA)	N/A
Proprietary HBM IP	HBM3 + HBM3E Silicon-proven at 4nm; 2 tapeouts confirmed	None Design services only; no memory interface IP
Business Model	Technology Owner IP licensing: scalable, near-zero marginal cost	Design Services Engineering time & materials; lower margin ceiling
Arm Token Access (May 2026)	AFA One of first 3 Malaysian firms; May 11 ceremony	AFA One of first 3 Malaysian firms; May 11 ceremony

Source: SkyeChip, Oppstar, Arm, Apex Securities

Thesis 6: Arm Flexible Access (AFA)- Unlocking World-Class Architecture

On 11 May 2026, SKYECHIP was formally presented with an offer letter for access to Arm's Flexible Access (AFA) programme, one of the first three Malaysian chip design firms to receive such an offer, alongside GreatAsic Technology and Oppstar Technology. The offer letters were presented during a ceremony officiated by Economy Minister Akmal Nasrullah Mohd Nasir, underscoring the national strategic significance of the initiative. On 23 June 2026, SkyeChip signed the definitive agreement for AFA access with MIDA, becoming the second of the three recipients to formalise its access (after Oppstar on 25 May 2026), and granting full access to Arm's chip design platform for product experimentation and development without upfront licensing fees.

The access tokens form part of the Malaysian government's USD250m (c.RM1.0bn) decade-long deal with Arm Holdings (backed by SoftBank), inked in March 2025. The initiative offers two access tiers: (i) Arm Flexible Access (AFA), tailored for start-ups and smaller companies, providing early, low-cost access to Arm's chip designs for experimentation, development, and testing without full upfront licensing fees; and (ii) Arm Neoverse Compute Subsystems (CSS), intended for larger, more established enterprises, providing ready-made chip building blocks that enable faster processor design. **A total of 25 AFA tokens and 7 CSS tokens have been allocated, with further recipients to be announced in due course.**

What is AFA? Arm Flexible Access is a low- to no-cost subscription model that gives companies early access to a broad portfolio of Arm's IP, including CPU cores (Cortex-A and Cortex-M series), GPU designs (Mali), interconnect IP (CoreLink/AMBA), security IP (TrustZone), and development tools without requiring full licensing fees upfront. Companies can experiment, design, and develop silicon using Arm's architecture during the development phase, with licensing fees triggered only when a chip moves into production. This dramatically lowers the barrier to entry for custom chip design, particularly for companies that are building their first Arm-based products.

With the AFA definitive agreement now executed, SkyeChip has full access to Arm's chip design platform and can begin developing Arm-based solutions immediately. The CSS platform, which grants access to Neoverse server-grade compute subsystems for high-performance CPU and AI platform development, remains at the conditional approval stage (received 14 April 2026), with the Group still evaluating the terms and conditions of the definitive agreement given the scale of

the undertaking and the costs involved. The receipt of conditional CSS approval validates SkyeChip's technical credibility and positions the Group to potentially develop high-performance Arm-based CPU and AI platforms, subject to finalisation of the definitive agreement.

The strategic implications are now more tangible with the AFA agreement signed. SkyeChip can begin developing Arm-based solutions for low-power and cost-optimised applications, specifically IoT and edge computing products, that integrate its existing memory interface IP and NoC IP with Arm's CPU cores. AFA, as confirmed in SkyeChip's prospectus, is targeted at "low-power and cost-optimised areas... smart IoT and edge computing solutions." The development of high-performance CPU and AI platforms requires CSS access, for which SkyeChip has conditional approval, with **c.RM82.0m** of IPO proceeds ring-fenced for this purpose. In the event the CSS definitive agreement is not finalised, SkyeChip has indicated it will pursue alternative approaches including RISC-V-based CPU solutions or custom AI hardware accelerators.

National Policy Endorsement. The government's signalling could not be clearer. Economy Minister Akmal Nasrullah Mohd Nasir, in his remarks at the 11 May 2026 ceremony, stated that the objective of the Silicon Vision initiative is to seed 10 local chip companies expected to collectively generate up to **c.USD20bn** in annual revenue and produce Malaysian-designed chips within five to seven years, with his personal target set at three years. As one of only three initial recipients of Arm access tokens, and now one of two to have signed definitive AFA agreements (alongside Oppstar), SkyeChip is positioned at the forefront of Malaysia's "Made by Malaysia" semiconductor ambitions. This is a meaningful strategic endorsement that reinforces SkyeChip's positioning within national semiconductor policy and may translate into further policy support, including the pending Pioneer Status renewal and future token allocations.

Forecasts. We have not included any revenue from AFA or CSS-related products in our base case forecasts, given that the CSS definitive agreement remains pending as at the LPD. However, we view the AFA execution as a meaningful de-risking event and the conditional CSS approval (received 14 April 2026) as credible medium-term optionality not currently priced into our valuation. For illustrative purposes, assuming 2-3 Arm-based contracts at an average value of **c.RM7m** each, the incremental revenue opportunity could reach **RM14-21m** per annum from FY28-FY29F onwards (**5-8%** upside to our FY28F revenue estimate), lifting our mid-FY28F Core EPS from 6.1 sen toward 6.4-6.5 sen and implying a fair value of **RM4.90-4.98** under **our 76.6x target multiple (5-7% upside to our TP of RM4.67)**, though this remains contingent on finalisation of the CSS definitive agreement, successful development and silicon validation, and customer adoption. The RM82.0m of IPO proceeds ring-fenced for CSS-based development (23.3% of gross proceeds) underscores the scale of management's ambition, and if successfully executed, would transform SkyeChip from a pure IP licensor into a silicon product company. The signing of the AFA definitive agreement on 23 June 2026 removes one layer of uncertainty and confirms the programme is progressing through execution, with the CSS resolution remaining the key outstanding catalyst. Any upside from Arm-based products would represent a catalyst for re-rating beyond our current fair value estimate of RM4.67, and we will revisit our estimates when formal development arrangements are announced.

Figure 12: Arm AFA & CSS - What SkyeChip Gets Access To

Component	Description	SkyeChip Access	Benefit
AFA - Arm Flexible Access Current Confirmed Access			
CPU Cores	Cortex-M0 to Cortex-A55 (IoT / Edge)	AFA Confirmed	IoT & edge compute products
GPU	Arm Mali (mainstream / IoT)	AFA Confirmed	Low-power graphics & ML
Interconnect	CoreLink / AMBA	AFA Confirmed	Complements SkyeChip's NoC IP
Security IP	TrustZone, CryptoCell	AFA Confirmed	Adds security capability
Dev Tools	Arm Development Studio + online training	AFA Confirmed	Accelerates design cycle
CSS - Neoverse Compute Subsystem Conditional Approval Only (Definitive agreement not yet signed RM82m ring-fenced)			
Server CPU	Neoverse V3 / N2 (cloud / AI / HPC)	Conditional Only	High-performance CPU platform
Mesh Interconnect	CMN - Coherent Mesh Network	Conditional Only	Server-grade interconnect
Full System IP	Power management, security, software stack	Conditional Only	Complete server SoC platform

Source: ARM, Malaysian Silicon Vision, Apex Securities

Investment Risks

Geographic Concentration. China and Taiwan together accounted for c.73.8% of FY26 revenue (China: 62.6%, Taiwan: 11.2%), a notable improvement from 90.6% in FPE Oct 2025, driven by the successful emergence of the US as 23.1% (RM35.8m) of FY26 revenue and South Korea as a new market at 1.0%. Q4 FY26 alone saw US revenue of RM28.9m (49% of Q4 revenue), underscoring rapid geographic rebalancing. Nevertheless, China remains the single largest market at **c.62.6%** of FY26 revenue, and any expansion of US export controls to cover silicon IP licensing could materially impact the Group. Vietnam operations launched in December 2024 provide additional diversification, but China geographic concentration, while improving, remains elevated.

Tax Exemption Uncertainty. The Section 127(3A) Pioneer Status exemption, which kept the effective tax rate at **c.2.5-2.9%**, expired on 9 September 2025. The renewal application was submitted to MIDA on 9 June 2025 and remains under review with no guaranteed outcome. Notably, the FY26 actual effective tax rate came in at just 3.0% (vs the prospectus guidance of approximately 5.0% or less), better than anticipated, reflecting: (i) the exemption covering the majority of FY26; and (ii) Vietnam operations benefiting from a 5-year corporate income tax exemption commencing May 2025. In the event the MIDA renewal is denied, the Group has indicated it will apply for Malaysian Digital (MD) tax incentives from MDEC as a fallback, which would limit the effective rate to approximately 12% on qualifying income. We estimate that a normalised 24% tax rate scenario, representing a true worst case, would reduce FY27F PAT by approximately 19% from RM90.2m to RM73.3m and EPS from 5.02 sen to 4.08 sen. We do not consider this our base case given the strength of the policy signals (SkyeChip is one of only three Arm AFA token recipients under the national Silicon Vision initiative, with conditional CSS approval received 14 April 2026), the Vietnam tax shield covering an estimated 12-15% of Group profit regardless of the Malaysian outcome, and the MD incentive fallback pathway that would cap the effective rate well below the full statutory level.

Customer Concentration and Contract Visibility. In FY26, customer concentration improved: 2 customers contributed 10% or more of revenue (total RM47.4m), down from 3 customers (RM72.2m) in FY25, while the total customer base nearly doubled to 26 (from 14 in FY25). The unbilled orderbook of **RM130.3m as at 31 March 2026 provides approximately 10 months of revenue visibility, representing a book-to-bill of 0.84x FY26 actual revenue of RM155.0m (down from 1.1x FY25 revenue), offset by the significantly expanded customer base.** The Group's revenue model is explicitly project-based rather than subscription-based, requiring continuous contract wins to sustain growth. The orderbook comprises RM52.3m from silicon IP

and RM78.0m from custom ASIC and other segments, with c.73% (RM94.6m) expected to be recognised in FY27.

Competition with Global Incumbents. Synopsys, Cadence, and Arm dominate the global semiconductor IP market at 10-100x SkyeChip's scale and R&D budgets, Synopsys alone generates **c.USD7.0bn** in annual revenue versus SkyeChip's **RM119.5m** (~USD26m). While SkyeChip competes in niche memory interface and NoC segments where global giants have comparatively less focus and structurally benefits from Chinese customers' preference for non-US, geopolitically neutral IP suppliers any aggressive move by incumbents into SkyeChip's core segments, or normalisation of US-China trade relations that removes the geopolitical premium, could intensify pricing pressure and reduce the Group's competitive advantage.

Dependence on Key Personnel and Talent. The Group's competitiveness is heavily dependent on its technical leadership including CTO Teh Chee Hak, formerly Chief Architect at Intel Microelectronics and its 365-strong IC design and technical team. Penang hosts major design centres for Intel, Broadcom (Avago Technologies), Infineon, and Renesas, creating fierce competition for experienced semiconductor engineers. The Group operates structured training programmes requiring each engineer to complete 110 hours across 25 modules within their first year, and has expanded into Vietnam where 19 employees have been hired as at the LPD with a target of 90 by end-2026 partly to access a wider talent pool. Loss of key personnel, particularly the founding technical team, could materially impair the Group's ability to sustain its IP development roadmap.

New Customer Survival Risk. Several of SkyeChip's customers are early-stage AI chip companies with uncertain product commercialisation timelines and volume ramp profiles. The Group's focus on upfront licensing fees, rather than volume-based royalties partially mitigates this risk by front-loading revenue recognition before customer products enter production. However, customer attrition among new accounts, or a broader slowdown in Chinese AI chip investment, remains a tail risk to earnings visibility.

Company Background

History and Founding Story.

SkyeChip Berhad (SKYECHIP) was incorporated in Malaysia in 2019 by co-founders Dato' Fong Swee Kiang and Teh Chee Hak, who will retain a combined 48.0% stake post-IPO. The Group was established in Penang, Malaysia's longstanding semiconductor hub, home to major design centres operated by Intel, Broadcom (Avago Technologies), Infineon, Renesas, and other multinational chipmakers, with the thesis that rising chip design complexity would drive structural demand for licensed, silicon-proven IP blocks from specialist providers. Rather than compete in chip manufacturing or traditional OSAT services where Malaysia already had an established presence, the founders chose to target the upstream, higher-value segment of the semiconductor value chain: the design and licensing of IP itself.

The Group's early years were spent building its engineering team and developing its first generation of memory interface IP (DDR and LPDDR) and Network-on-Chip IP. By FY23, SkyeChip had achieved RM57.2m in revenue and RM28.6m in net profit, demonstrating commercial viability. A rapid growth phase followed as the portfolio expanded into HBM3 and HBM3E interfaces at advanced process nodes, while simultaneously launching the custom ASIC segment in September 2023. Revenue grew at a 44.6% CAGR from FY23 to FY25, reaching RM119.5m. The momentum accelerated further in FY26, with the Group delivering RM155.0m in revenue (+29.7% YoY), RM48.5m in PAT (+35.0% YoY), and an improved gross margin of 45.1% (vs 42.2% in FY25), while nearly doubling its customer base from 14 to 26 and successfully penetrating the US market (23.1% of FY26 revenue).

The IPO marks the next phase of the Group's development. The RM352m in gross proceeds will be deployed primarily into R&D - including next-generation HBM4, LPDDR6, RISC-V, and

automotive IP development, as well as expansion of computing infrastructure, EDA tools, and operational facilities. The Group has also received a formal offer letter for Arm Flexible Access (AFA) on 11 May 2026 under the Malaysian government's US\$250m Arm initiative, positioning it among the first three Malaysian companies with access to Arm's IP architecture.

Figure 13: Key Milestones

Year	Milestone
2019	Incorporation in Penang, Malaysia; Registration No. 201901014484
FY23	Revenue exceeds RM57.2m; net profit RM28.6m; standard silicon IP established as core segment
FY24	Custom ASIC segment launched (September 2023); revenue grows 34.8% to RM77.1m; HBM3 IP commercialised
FY25	Revenue reaches RM119.5m (+55% YoY); HBM3E IP commercialised - silicon first-time success at 4nm / 8,800 Mbps
Jan 2025	Joins Intel Foundry Accelerator IP Alliance - access to Intel Foundry's advanced process technologies
Dec 2024	Vietnam operations established (SkyeChip HCMC and SkyeChip Da Nang)
Sep 2025	RISC-V SoC contract secured; Section 127(3A) Pioneer Status tax exemption expires; renewal submitted to MIDA
Apr 2026	Prospectus launched; conditional approval received for Arm AFA and Arm Neoverse CSS platforms
11 May 2026	Formal AFA offer letter received - one of first three Malaysian firms under Malaysia-Arm US\$250m initiative
20 May 2026	Listing on Main Market of Bursa Malaysia at RM0.88 per share

Source: Company, Apex Securities

Management Team and Key Personnel

The Group's competitive position is inseparable from the calibre of its technical and management team. In the semiconductor IP industry, the quality of IP output is directly determined by the expertise and experience of the engineers who design it - there is no manufacturing process or distribution network to fall back on. SkyeChip's team is drawn primarily from Penang's deep pool of semiconductor talent, with key personnel holding prior experience at multinational chipmakers.

Dato' Fong Swee Kiang: Co-Founder and Executive Director (24.0% post-IPO stake). Dato' Fong oversees the Group's strategic direction, business development, and stakeholder relationships. His role is primarily commercial and strategic, complementing the technical leadership of co-founder Teh Chee Hak. The co-founders' combined 48.0% post-IPO stake, coupled with the absence of any offer-for-sale component in the IPO represents one of the strongest founder alignment structures we have seen in a recent Malaysian listing.

Teh Chee Hak: Co-Founder, Executive Director and CTO (24.0% post-IPO stake). Mr Teh is arguably the Group's most critical asset. He previously served as chief architect at Intel Microelectronics (Penang), where he was responsible for the architecture and microarchitecture of FPGA products and IPs across a 20-year tenure spanning Intel Microelectronics and Altera Malaysia (2000–2020). His transition from Intel, where he led architecture for programmable logic devices, to founding a memory interface and NoC IP company reflects a deliberate bet on the convergence of high-speed interface design and AI-driven demand for HBM. His credibility within the global semiconductor IP community is a meaningful intangible asset: customers licensing critical IP for chips costing tens of millions of dollars to tape out place significant weight on the technical reputation of the IP provider's leadership.

Engineering team. The Group's technical team comprises 365 professionals as at the LPD, with expertise spanning memory interface design (DDR, LPDDR, HBM), network-on-chip architecture, die-to-die interconnect, physical design, verification, and firmware development. The team operates primarily from the Penang headquarters, with a growing R&D presence in Vietnam. The Group has implemented a structured onboarding programme requiring each engineer to

complete 110 hours of training across 25 modules within their first year, covering advanced IC design and verification across digital and analogue VLSI methodologies.

Board composition. Beyond the two co-founders, the Board comprises an Independent Non-Executive Chairman and three Independent Non-Executive Directors, all appointed in February 2025 ahead of the IPO. The Chairman, Dato' Seri Wong Siew Hai, brings 28 years of Intel Malaysia seniority, including as VP & Country Managing Director and currently serves as President of the Malaysia Semiconductor Industry Association, adding meaningful industry credibility and policy connectivity. The audit and governance function is anchored by Datuk Alexandra Chin, a 40-year accounting veteran and former global ACCA President (2015–16), and Norinne Ira Dewal, a corporate lawyer specialising in capital markets and M&A. Industry and operational depth is provided by Dato' Seri Gooi Soon Chai, former SVP of Keysight Technologies (NYSE). We view the Board's composition as appropriate for a company at SkyeChip's stage - bringing semiconductor industry credibility, financial governance, and legal expertise. The key post-listing dynamic to monitor will be whether the Board's independence is sufficient to provide effective oversight of the founding management team as the Group scales and takes on the obligations of a Main Market-listed company.

Figure 14: Key Management Team

Executive Directors			
Dato' Fong Swee Kiang	<i>Co-Founder · Executive Director & CEO</i>	24.0%	35+ yrs semiconductor · Ex-Director, Intel Penang Design Center · Ex-VP, Altera Malaysia · Ex-Sr Director, Broadcom
Teh Chee Hak	<i>Co-Founder · Executive Director & CTO</i>	24.0%	20+ yrs semiconductor · Ex-Chief Architect, Intel Microelectronics & Altera (2000–2020) · Leads IP & ASIC strategy
Independent Non-Executive Chairman			
Dato' Seri Wong Siew Hai	<i>Independent Non-Executive Chairman</i>	—	28 yrs Intel Malaysia · Retired VP, Global Assembly Test Manufacturing · President, MSIA (2021–present)
Independent Non-Executive Directors			
Dato' Seri Gooi Soon Chai	<i>Independent Non-Executive Director</i>	—	35+ yrs HP / Agilent / Keysight (NYSE) · Retired SVP, Keysight (2025) · Director, ViTrox (Bursa) & Frencken (SGX)
Datuk Alexandra Chin	<i>Independent Non-Executive Director</i>	—	40+ yrs accounting & audit · Ex-Global President, ACCA (2015–16) · Director, Suria Capital (Bursa)
Norinne Ira Dewal Binti Md Ali	<i>Independent Non-Executive Director</i>	—	20+ yrs corporate & commercial law · M&A, capital markets & securities regulation · Partner, Wei Chien & Partners

Source: Company, Apex Securities

Organisational Structure and Subsidiaries.

SKYECHIP operates as an investment holding company, with all operational activities conducted through six wholly-owned subsidiaries spanning four countries. This structure reflects the Group's deliberate strategy of locating design capabilities close to key customer markets while maintaining centralised IP ownership and technical direction from the Penang headquarters.

SkyeChip Technology Sdn Bhd (Malaysia) is the principal operating subsidiary and the technical heart of the Group. Based in Penang, it houses the core IC design team responsible for the development, verification, and commercialisation of all silicon IP and ASIC products. Penang was chosen as the Group's base for good reason: the state hosts one of Southeast Asia's densest concentrations of semiconductor talent, with Intel, Broadcom (Avago Technologies), Infineon, Renesas, AMD, and other multinationals operating major design centres within a 20km radius. This ecosystem provides SKYECHIP with access to a deep pool of experienced IC designers while also creating the competitive talent dynamic noted in our risk section.

SkyeChip Semi Sdn Bhd (Malaysia) supports the Group's domestic business development, customer engagement, and administrative functions. It also serves as the contracting entity for certain Malaysian government-related initiatives, including the Group's participation in the National Semiconductor Strategy (NSS) and the Arm Flexible Access programme.

SkyeChip China serves the Group's largest single market, with China accounting for 62.6% of FY26 revenue (down from 73.3% in FPE Oct 2025, reflecting geographic diversification into the US and South Korea). The subsidiary manages customer relationships with Chinese fabless IC companies, primarily AI chip designers based in Shanghai, Guangzhou, Hefei, and Shenzhen and

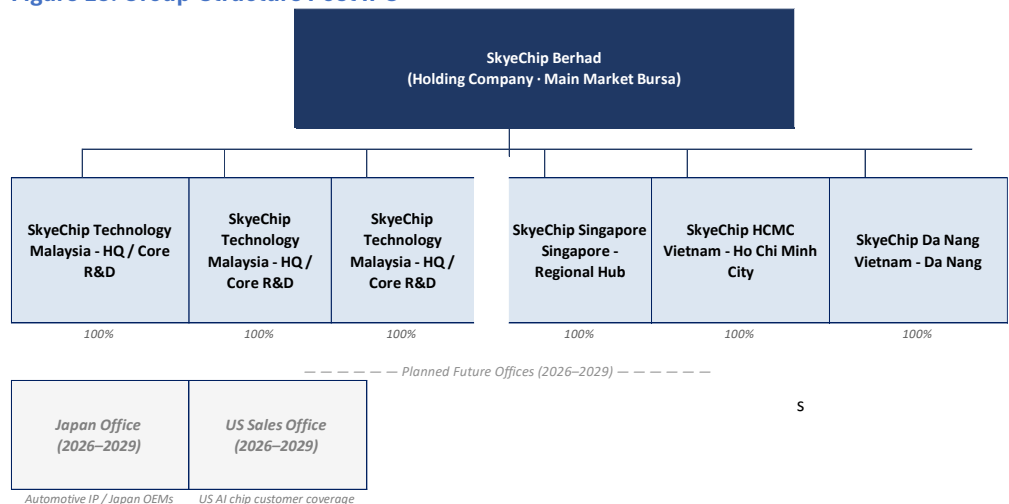
provides localised technical support and integration services. The strategic rationale for a direct Chinese presence is clear: proximity to customers accelerates the IP evaluation and integration process, which typically involves intensive technical collaboration between SKYECHIP's engineers and the customer's chip design team. Given the geopolitical sensitivity of the China market, the subsidiary also serves as a buffer that keeps customer-facing commercial activities within the Chinese jurisdiction while IP ownership and core R&D remain domiciled in Malaysia.

SkyeChip Singapore provides a regional hub to serve Singaporean and broader Southeast Asian customers. Singapore's role as a regional semiconductor and financial centre makes it a natural base for engaging customers across ASEAN, as well as for interfacing with global EDA vendors and foundry partners, several of whom maintain significant Singapore operations.

SkyeChip HCMC and SkyeChip Da Nang (Vietnam) represent the Group's most significant operational expansion outside Malaysia. Established in December 2024, the Vietnam operations currently employ 19 staff as at the LPD but are expected to scale rapidly to 90 by end-2026. Management has guided that Vietnam will contribute **c.12-17% of FY27 revenue**, primarily through outsourced IC design services that complement and extend the Penang-based core team's capacity. Vietnam offers two strategic advantages: (i) a growing pool of engineering talent at salary levels below equivalent Penang-based roles, providing meaningful cost arbitrage as the Group scales its engineering headcount, and (ii) access to a wider talent pipeline, partially mitigating the competitive pressure for semiconductor designers in Penang. The decision to establish two offices, in Ho Chi Minh City and Da Nang suggests the Group is casting a wide net across Vietnam's two main technology hubs to maximise talent access.

Future expansion. The Group plans to establish and/or expand R&D and sales offices in Japan and the US between 2026 and 2029. The US sales office would support distribution of silicon IP and silicon products to American customers, where the Group currently generates **c.23.1%** of FPE revenue, a nascent but strategically important market given the US's role as the world's largest semiconductor end-market. The Japan office would provide access to Japanese semiconductor companies and automotive OEMs, aligning with the Group's planned expansion into automotive silicon IP. Both offices are budgeted within the **RM19.0m** allocation for expansion of operational facilities and resources under the IPO proceeds utilisation.

Figure 15: Group-Structure Post IPO



Source: Company, Apex Securities

Figure 16: Post-IPO Shareholding Structure

Shareholder	Stake (%)	Category
Dato' Fong Swee Kiang	24.0	<i>Co-Founder</i>
Teh Chee Hak	24.0	<i>Co-Founder / CTO</i>
SKC Team 2	7.9	<i>ESSPP SPV</i>
SKC Team / SKC Team 1 / SKC Team 3	6.2	<i>ESSPP SPV</i>
Lion X	3.8	<i>Pre-IPO Investor</i>
iC Capital Management	3.6	<i>Pre-IPO Investor</i>
Areca Capital	3.5	<i>Pre-IPO Investor</i>
InterVest	3.3	<i>Pre-IPO Investor</i>
Gobi	1.4	<i>Pre-IPO Investor</i>
PIV Perkasa	0.4	<i>Cornerstone Investor</i>
Public & non-public shareholders	21.9	<i>Post-IPO Public</i>
Total	100.0	

Source: Company, Apex Securities

Business Model

Silicon IP Licensing - The Core Profit Engine.

As discussed in the investment thesis, silicon IP licensing represents **77.0% of FY26 revenue (silicon IP segment: RM119.4m)** revenue across two sub-segments:

- (i) **Standard silicon IP (part of the 77.0% silicon IP segment in FY26).** Off-the-shelf catalogue products designed to industry standards and licensed across multiple customers simultaneously. This sub-segment comprises three product families: memory interface IP (58% of FPE revenue), Network-on-Chip IP (16%), and Die-to-Die interface IP (5%). The scalability of standard silicon IP is the defining characteristic of SkyeChip's business model, once a design is silicon-proven and validated, each additional licence generates near-pure profit with minimal incremental cost, as the core R&D expenditure has already been incurred.
- (ii) **Custom silicon IP (included within the silicon IP segment in FY26; previously 11.1% of FPE revenue).** Bespoke modifications of existing standard IP blocks tailored to individual customer specifications. This includes multi-interface protocol IPs supporting DDR, LPDDR, MIPI, LVDS, and multi-standard I/O interfaces. Custom silicon IP was the Group's largest revenue contributor in FY23 (55.4% of revenue, RM31.7m), reflecting the Group's early reliance on bespoke project work before the standard IP catalogue achieved commercial scale. The segment has since declined significantly in revenue share to 36.6% in FY24, 9.2% in FY25, and 11.1% in FPE Oct 2025, as standard silicon IP licensing has grown rapidly and become the dominant revenue driver. In FY26, the combined silicon IP segment (standard + custom) contributed RM119.4m or 77.0% of total revenue, growing 39.3% YoY from RM85.7m. This mix shift towards standard IP is structurally positive: standard silicon IP carries higher margins, is more scalable, and generates recurring licensing income across multiple customers, whereas custom silicon IP is inherently project-specific and less repeatable. ***The declining share of custom silicon IP in total revenue should therefore be viewed as a sign of business model maturation rather than segment weakness.***

Licensing mechanics. The typical engagement involves: (i) an evaluation phase where the customer assesses IP against technical requirements, (ii) a licensing agreement with an upfront access fee structured as a fixed lump-sum contract, and (iii) integration support where SkyeChip's engineers assist with incorporating the IP and resolving integration challenges. Unlike Arm, which derives significant revenue from per-unit royalties, SkyeChip focuses on upfront

licensing, a pragmatic approach given the early-stage nature of many customers and uncertain production volumes. **This front-loads revenue recognition but foregoes participation in customer production upside, a trade-off that may evolve as the customer base matures.**

Custom ASIC Design - Growth Accelerator (22.3% of FY26 Revenue)

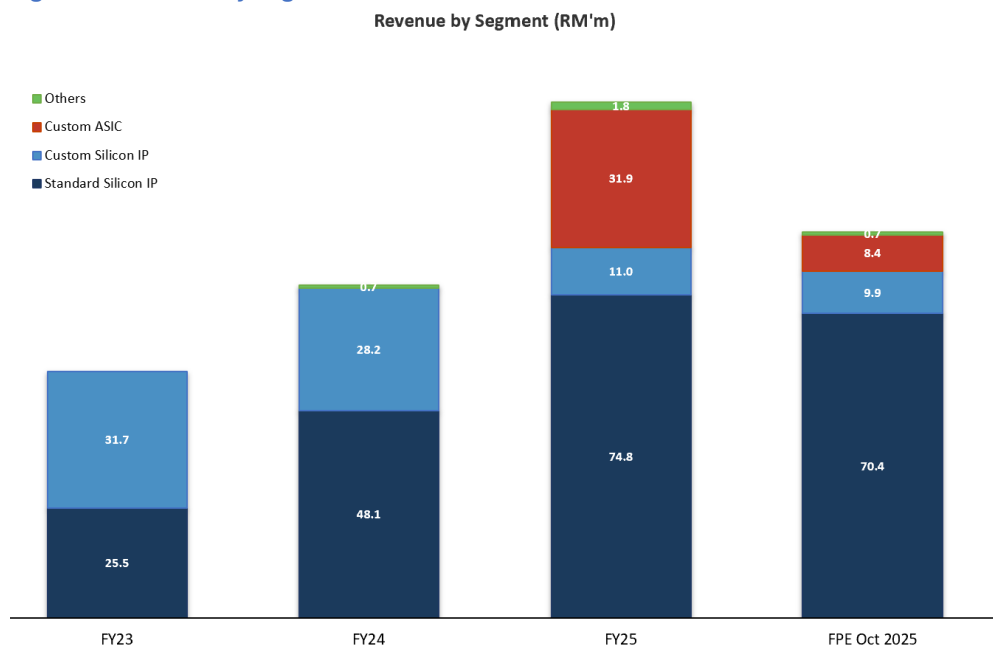
The Custom ASIC segment provides full-chip design services for application-specific integrated circuits tailored to specific customer requirements - primarily IoT processors and AI inference chips. The segment launched in September 2023, grew rapidly to 26.7% of FY25 revenue (RM31.9m), appeared to moderate to 9.4% in FPE Oct 2025, but recovered to 22.3% (RM34.6m) of FY26 revenue, representing 8.3% YoY growth. The ASIC segment has proven more resilient and recurring than the FPE data initially suggested. The investment thesis covers the strategic rationale and ASIC-to-IP cross-selling dynamic in detail.

Expansion pipeline. The Group plans to expand ASIC offerings through joint-development arrangements with technology partners targeting custom compute and AI hardware accelerators, though no formal arrangements have been concluded as at the LPD. Additionally, the Group is developing capabilities in: (i) 2.5D/3D I/O chiplets - including memory I/O chiplets, D2D interconnect chiplets, and chiplet-based accelerators; (ii) compute-in-memory (CIM) silicon dies integrating computational capabilities directly within or near the memory chip, eliminating the need for data transfer between memory and processing units; and (iii) automotive silicon IP targeting ADAS and autonomous driving applications with ISO26262 compliance, with commercial contributions expected between 2026 and 2027 on a licensing basis. These product lines remain at an early development stage and are not reflected in our base case forecasts.

Others (0.6% of FY26 Revenue)

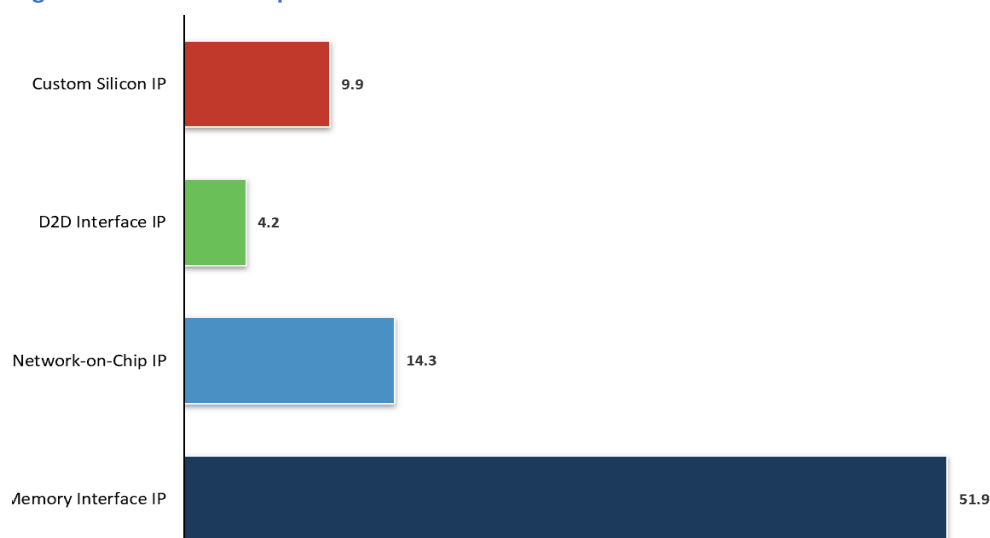
The Others segment comprises IC and PCB design services provided on a by-request basis, memory test system design, and engineering services supporting custom ASIC product development. This segment is not a strategic priority and is expected to remain a small proportion of Group revenue. FY26 Others revenue was RM1.0m (0.6%), broadly consistent with prior periods

Figure 17: Revenue by Segment



Source: Company, Apex Securities

Figure 18: Revenue Composition within Silicon IP



Source: Company, Apex Securities

Supply Chain and EDA Dependencies

The Group's cost structure is dominated by two categories: personnel costs (IC designer salaries and benefits) and EDA tool and verification IP subscriptions, together accounting for the majority of operational expenditure.

EDA tools. The Group's major EDA suppliers include Synopsys (Ireland), Siemens (Singapore), and Ansys (USA). Synopsys tools procured directly or through ICE, the sole Malaysian distributor for Synopsys have been the Group's core design toolchain since 2020, covering logic, circuit, and physical design. Siemens provides IC verification and design-for-manufacturability tools. Ansys provides specialised IC package design tools covering signal integrity, power delivery, and reliability simulation. Importantly, Ansys was acquired by Synopsys in July 2025, meaning two of the three named EDA suppliers are now part of the same corporate group, a concentration risk the Group has begun to mitigate by onboarding Cadence as an alternative EDA provider as at the LPD. EDA tool and verification IP subscriptions collectively accounted for **c.60.6%** of total operational costs and **c.7.3%** of cost of sales in FPE Oct 2025 (expected to remain broadly similar in FY26).

In-house EDA development. The Group is developing RAPTuner, a proprietary network architecture simulation and optimisation tool designed to support NoC IP integration. Currently bundled with its NoC IP offering at no additional charge, RAPTuner has longer-term standalone monetisation potential as a licensed EDA product. We have not included any RAPTuner licensing revenue in our base case forecasts.

Outsourced design services. VNCHIP Technology Joint Stock Company (Vietnam) provides outsourced IC design services, accounting for c.8.2% of total operational costs and c.1.0% of cost of sales in FPE Oct 2025 (the most recent period for which detailed cost breakdowns are available), providing flexible capacity to manage workload fluctuations.

Computing infrastructure. ICE (Malaysia) the sole Synopsys distributor in Malaysia, provides servers, storage, and high-performance computing resources as well as EDA tool procurement. The RM38.1m IPO proceeds allocation for computing infrastructure reflects the significant and growing compute requirements as the Group moves into more complex IP at advanced process nodes.

Figure 19: Major Suppliers FPE OCT 2025

Supplier	Country	Products / Services
ICE (incl. Synopsys / Ansys via ICE)	Malaysia	EDA tools, verification IP, computing infrastructure (Sole Synopsys distributor in Malaysia; also procures Ansys tools)
Siemens	Singapore	EDA tools, verification IP (within combined ICE/Synopsys figure above)
Synopsys	Ireland	EDA tools, verification IP — direct procurement (also parent of Ansys since July 2025)
VNCHIP Technology Joint Stock Co.	Vietnam	Outsourced IC design services

Source: Company, Apex Securities

Revenue Recognition and Contract Structure

The Group recognises revenue under MFRS 15 over time as performance obligations are satisfied measured by proportion of design work completed for silicon IP, and by project milestones for custom ASIC. Upfront fees received before obligations are met are recorded as contract liabilities. ASIC contracts carry milestone-linked billing tied to design deliverables architecture sign-off, RTL completion, verification closure, and tape-out. Silicon IP contracts are structured as fixed lump-sum agreements with revenue recognised over the design and integration period.

As at 31 March 2026, the unbilled orderbook stood at **RM130.3m** across 18 contracts, a book to bill ratio of 1.1x FY25 revenue comprising RM52.3m from silicon IP and RM78.0m from custom ASIC. Of this, c.RM94.6m (73%) is expected to be recognised in FY27, with the remaining RM35.7m in FY28–29. The Group's customer base consists exclusively of fabless IC companies engaged through direct distribution, with the longest-standing relationship spanning six years.

Figure 20: Orderbook Composition and Recognition Schedule

Headline Metrics	
Total unbilled orderbook (as at 31 Mar 2026)	RM130.3m
Number of contracts	18
Cover ratio (vs FY25 revenue of RM119.5m)	1.1x
Composition by Segment	
Silicon IP component	RM52.3m (40%)
Custom ASIC + Others component	RM78.0m (60%)
Revenue Recognition Timeline	
Expected recognition in FY27	RM94.6m (73%)
Expected recognition in FY28–29	RM35.7m (27%)

Source: Company, Apex Securities

Industry Overview

The Global Semiconductor Industry - On Track for USD1 Trillion

The global semiconductor industry is entering an unprecedented expansion phase. According to the World Semiconductor Trade Statistics (WSTS), global semiconductor sales reached USD795.6bn in 2025, a **c.26.2% year-on-year increase**, one of the strongest annual expansions in the industry's history, confirmed independently by the Semiconductor Industry Association

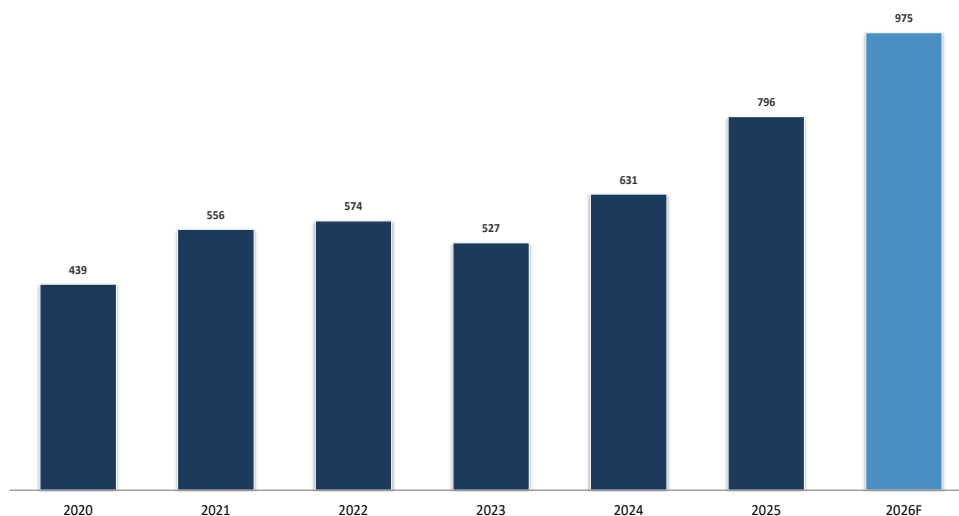
(SIA) at USD791.7bn / **+25.6%** using its three-month moving average methodology. Growth accelerated through the year, with Q4 2025 revenues of **USD238.9bn up 38.4%** versus Q4 2024 (WSTS) or USD236.6bn / +37.1% per SIA, reflecting minor methodological differences. By product category, logic devices generated USD301.9bn (+39.9% YoY) and memory products followed at USD223.1bn (+34.8% YoY) both driven overwhelmingly by AI-related demand.

Looking ahead, WSTS forecasts the global semiconductor market to reach USD975bn in 2026 with Q1 2026 already recording USD298.5bn in sales, up 25% from Q4 2025, confirming the industry remains firmly on track. SIA President and CEO John Neuffer stated: "global sales in 2026 are projected to reach roughly USD1 trillion." **Memory and logic are again expected to lead, growing by 39.4% and 32.1% respectively in 2026.**

The AI-driven component of this expansion is particularly significant for SkyeChip. Deloitte initially estimated the AI chip market in 2026 at **c.USD300bn**, but following the December 2025 upward revision of USD175bn in the global chip market by WSTS (all of which was attributable to AI demand), Deloitte revised its AI chip estimate upward to **c.USD500bn** for 2026 representing approximately half of total global semiconductor revenue. This AI chip segment creates direct demand for the memory interface and interconnect IP that SkyeChip provides.

The industry is characterised by what we are calling a "giga cycle", a structural supercycle distinct from traditional semiconductor cyclicality, driven by the convergence of AI infrastructure buildout, data centre expansion, automotive electrification, and IoT proliferation. While cyclical corrections remain possible, the consensus view is that AI-driven semiconductor demand represents a multi-year structural shift rather than a temporary demand spike.

Figure 21: Global Semiconductor Sales 2020–2026F (USD bn)



Source: SIA, WSTS, Apex Securities

The Semiconductor IP Market - Where SkyeChip Competes

Semiconductor intellectual property (IP) refers to pre-designed, pre-verified building blocks: commonly called "IP cores" or "IP blocks" that chip designers license and integrate into their system-on-chip (SoC) or ASIC designs. Rather than designing every functional component from scratch, chip designers license proven IP blocks from specialist providers, dramatically reducing cost, development time, and design risk. Over **c.52%** of semiconductor companies now license third-party IP for SoC integration, reflecting the structural shift toward IP-based chip design as complexity escalates and time-to-market pressures intensify (industryresearch.biz).

The market is segmented into four categories, each with distinct growth dynamics:

Processor IP (c.47% in 2023, declining toward ~41% by 2028) encompasses CPU, GPU, and AI accelerator cores. Arm Holdings dominates this segment globally. Processor IP remains the largest single category by revenue, driven by demand for high-performance processors in mobile, automotive, and AI applications. While processor IP remains the largest single revenue category, its share has structurally declined from 58% in 2017 to 47% in 2023, as interface IP has grown rapidly. IPnest forecasts processor IP to decline further to approximately **41%** by 2028 as interface IP takes share.

Interface IP (c.28% of market, fastest-growing segment) includes memory interfaces (DDR, LPDDR, HBM), high-speed serial links (PCIe, USB, Ethernet), and die-to-die (D2D) interconnects. This is the segment where SkyeChip operates. Interface IP is confirmed as the fastest-growing sub-segment across multiple research firms, driven by the "memory wall" problem: in modern AI systems, the bottleneck is increasingly not compute speed but the rate at which data can be moved between processors and memory. According to IPnest proprietary data, interface IP's market share has risen materially since 2017 a structural shift driven by the proliferation of HBM, advanced DDR standards, and chiplet-based architectures requiring die-to-die interconnect IP. Companies that master the data path, the memory interfaces, die-to-die links, and on-chip interconnect are ascending in strategic importance within the semiconductor ecosystem.

Memory IP (c.19% of market) covers embedded memory compilers, DRAM controllers, SRAM, and flash memory IP. Memory IP demand grew **c.22%** in 2024, supported by HBM proliferation and LPDDR adoption in mobile and automotive applications (industryresearch.biz).

Other IP (c.16%) includes analogue IP (11%), security IP, and physical IP (standard cell libraries, I/O pads). Within this category, automotive-grade IP with ISO 26262 certification represents 18% of new IP launches, a rapidly growing niche as the automotive industry electrifies and adopts advanced driver assistance systems (industryresearch.biz).

“Our View: SkyeChip's positioning at the intersection of interface IP and memory IP: the two segments with the strongest structural tailwinds from AI, is a key element of our investment thesis. For a detailed discussion, refer to Investment Thesis #1 (HBM IP) and Investment Thesis #2 (scalable licensing model)”

The Semiconductor IP Market - Size, Growth, and Regional Structure

Market sizing for semiconductor IP varies across research providers, reflecting different scope definitions and methodologies. We summarise the most widely cited estimates below. We take the midpoint and estimate the global semiconductor IP market at **c.USD8bn** in 2025, growing at **12.5%** CAGR through the next decade a wide range that reflects genuine methodological divergence rather than data uncertainty.

Figure 22: Global Semiconductor Sales 2020–2026F (USD bn)

Source	Market Size	Base Year	CAGR	Projected Size
Global Market Insights	USD 8.8bn	2024	15.1%	USD 35.7bn by 2034
ResearchAndMarkets	USD 10.2bn	2025	9.7%	USD 23.4bn by 2034
Precedence Research	USD 8.17bn	2025	8.52%	USD 17.1bn by 2034
MarketsandMarkets	USD 7.5bn	2024	8.5%	USD 11.2bn by 2029
Research Nester	USD 7.95bn	2025	7.5%	USD 16.4bn by 2035
The Insight Partners	USD 7.5bn	2025	10.2%	USD 17.3bn by 2034

Source: Various, Apex Securities

Within this market, interface IP SkyeChip's target segment is growing at **c.20%+ CAGR**, meaningfully outpacing the overall market average of **8–15%**. This is confirmed by IPnest proprietary data showing interface IP's revenue share rising from 18% of the total design IP market in 2017 to 28% in 2023, forecast to reach 38% by 2028, at the direct expense of processor IP, which has declined from 58% to 47% over the same period and is expected to decline further to 41% by 2028. The acceleration is driven by AI chip design activity requiring specialised IP for high-bandwidth memory access, low-power inference, and heterogeneous chiplet integration, precisely the segments where SkyeChip competes.

Regional distribution and Our View. Asia-Pacific leads the global semiconductor IP market with c.44% share, reflecting the region's vast semiconductor fabrication and design base with China, Taiwan, and South Korea as the primary contributors. North America holds c.32% share, driven by cloud computing, data centre investments, and the concentration of major AI chip designers. Europe accounts for c.17%, with particular focus on automotive IP integration driven by the EV transition and ADAS adoption (industryresearch.biz). SkyeChip's **c.62.6% in FY26 (down from 73.3% in FPE Oct 2025)** China revenue exposure positions it directly within the largest and fastest-growing regional semiconductor IP market - a structural tailwind further reinforced by Chinese IC designers' increasing preference for non-US IP suppliers in the current geopolitical environment.

The HBM IP Market - SkyeChip's Core Addressable Segment

The HBM IP market - comprising controller IP and PHY IP specifically for HBM interfaces represents the most directly relevant sub-segment of the semiconductor IP market for SkyeChip's valuation.

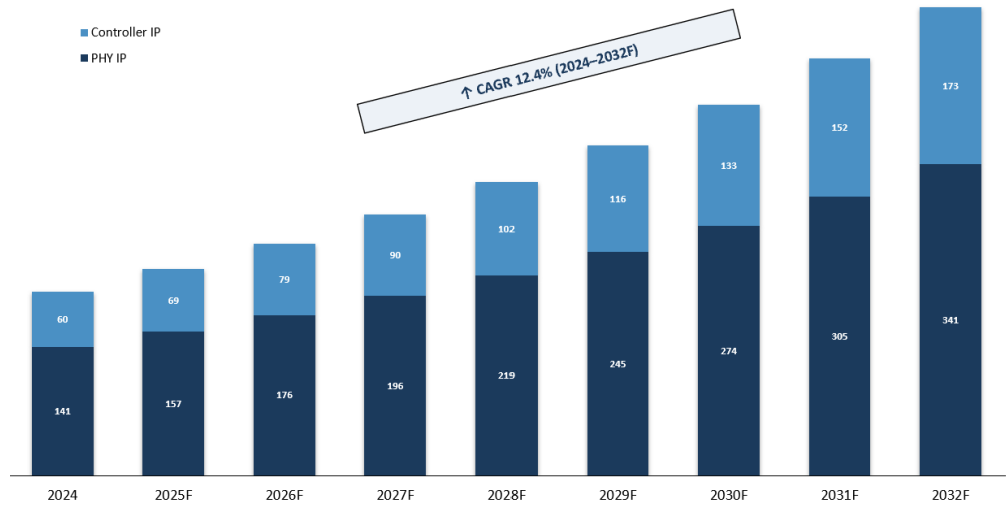
According to SNS Insider, the global HBM IP market was valued at **c.USD201.15m** in 2024 and is projected to reach **c.USD513.47m** by 2032, growing at a CAGR of **12.43%**. Within this, PHY IP held a dominant **c.70%** share in 2024, reflecting the critical importance of the physical layer in enabling high-speed data transfer between processors and HBM stacks. Controller IP is the fastest-growing sub-segment at a CAGR of **14.05%**, driven by increasing memory management complexity in AI accelerators. (SNS Insider, GlobeNewswire)

Servers accounted for **c.55%** of HBM IP demand in 2024, with the remainder distributed across networking, automotive, and consumer applications consistent with the broader AI infrastructure buildout driving demand for the highest-bandwidth memory architectures.

The competitive landscape for HBM interface IP is highly concentrated among a small number of specialist providers:

1. **Synopsys** - DesignWare HBM3/HBM3E/HBM4 PHY and Controller IP; the dominant global HBM interface IP provider, with wired interface IP representing approximately 71% of Synopsys' design IP revenue (IPnest, April 2024). Synopsys reported FY2025 total revenue of USD7.1bn (+15% YoY), with Design IP contributing USD1.75bn (24.8% of total). (Source: Synopsys, IPNest)
2. **Cadence** - DDR5/HBM3/HBM4E PHY and Controller IP; Cadence's interface IP portfolio covers the full spectrum of high-speed memory and serial link protocols. Cadence's IP business grew nearly 25% YoY in FY2025, driven by expanding adoption of HBM, UCIe, PCIe, DDR, and SerDes IP. Total FY2025 revenue: USD5.3bn (+14% YoY) (Source: Cadence)
3. **Rambus** - HBM3 PHY, CXL 3.0 controller, and DDR5 Memory Interface Chips (hardware); Rambus reported full year 2025 revenue of USD707.6m (+27.1% YoY), with record product revenue of USD347.8m (+41% YoY) driven by DDR5 memory interface chip demand and AI server build-out. (Source: Rambus FY2025 earnings)
4. **Alphawave Semi / Qualcomm** - AlphaCORE HBM and D2D SerDes IP; note that Alphawave Semi was acquired by Qualcomm in June 2025, bringing its wired connectivity IP portfolio under Qualcomm's ownership.

Figure 23: HBM IP Market Size - PHY IP vs Controller IP



Source: SNSInsider, Apex Securities

SkyeChip competes within this landscape as a niche specialist focused on HBM3/HBM3E PHY and controller IP, differentiated by its geopolitical positioning as a Malaysian-domiciled, non-US IP provider, its advanced-node silicon-proven track record (HBM3E at 4nm), and its specialised focus on memory interface and interconnect IP for the Chinese and Taiwanese AI chip design market.

For a detailed discussion of HBM technology, market dynamics, and SkyeChip's competitive position, refer to Investment Thesis #1: Only Commercialised HBM3/HBM3E IP House in ASEAN.

The AI Memory Interface Bottleneck

The fundamental driver of SKYECHIP's addressable market is the "memory wall" - the widening gap between processor compute speed and the rate at which data can be fed to the processor from memory. In AI workloads, this bottleneck is particularly acute: during large language model inference, the GPU must read the entire model weights plus the ever-growing key-value cache from HBM for every token generated. If memory bandwidth cannot deliver data at terabytes per second, the GPU sits idle regardless of its compute power. This makes most LLM inference workloads memory bandwidth-bound rather than compute-bound. We frame it as: memory is the new CPU, and without memory IP, compute units starve for data. AI scaling is increasingly constrained by data movement rather than compute alone, shifting the focus from raw GPU performance to memory bandwidth, interconnect efficiency, and packaging sophistication.

The industry's response has been to develop ever-faster memory interfaces - HBM3 (665-819 GB/s per stack), HBM3E (up to 1,200 GB/s per stack), and HBM4 (targeting ≥2,048 GB/s per stack) - each requiring increasingly sophisticated interface IP. NVIDIA's GPU roadmap illustrates the trajectory: HBM per chip has increased from 80 GB (H100) to 288 GB (Blackwell Ultra) to a planned ~512 GB (Rubin Ultra, based on NVIDIA GTC 2025 roadmap projections) - a **6.4x** increase over three generations. **Each successive generation requires memory interface IP of increasing complexity and speed.**

Our View. The memory wall is not a temporary phenomenon - it is a structural feature of AI computing that will intensify as models grow larger and inference demands scale. This creates a long-duration tailwind for memory interface IP providers like SKYECHIP, as the demand for ever-faster, more sophisticated interfaces is directly tied to the growth of AI computing itself.

Rising Chip Design Costs - The Structural Case for Licensed IP

For a detailed discussion of chip design cost escalation, refer to Investment Thesis #4: Deep Technical Moat.

The industry context is that design costs have escalated from c.USD48m at 28nm to c.USD590m at 3nm, with 2nm projected at USD725m+. Verification accounts for over 70% of total development cost (Cadence; Global Semiconductor Alliance). The global ASIC design services market is projected at **c.USD18.9bn in 2026, growing at a CAGR of 7.2% to USD30.7bn by 2033**, driven by custom chip demand in AI, 5G, and automotive applications, with this growth being structural rather than a one-off spike - accelerated by AI across full-custom, semi-custom, and programmable ASIC segments. (Source: Persistence Market Research)

The most compelling structural shift is the trajectory of custom ASIC adoption at hyperscale.

According to Counterpoint Research (January 2026), global data center AI server compute ASIC shipments are projected to triple by 2027 compared to 2024 levels, with ASIC shipments expected to surpass GPU shipments for the first time in history by 2028 - crossing 15 million units as the top ten AI hyperscalers deploy over 40 million custom AI chips cumulatively during 2024–2028. This is independently corroborated by TrendForce, which projects CSP in-house ASIC deployment to grow 44.6% in 2026 versus 16.1% for GPU-based servers.

Network-on-Chip (NoC) - The Interconnect Fabric

As chip designs integrate dozens to hundreds of functional blocks: CPU cores, GPU clusters, AI accelerators, memory controllers, security engines, and I/O interfaces - the on-chip communication fabric becomes a critical performance determinant. NoC IP replaces ad-hoc point-to-point wiring with a packet-based network, providing structured, scalable interconnect that routes data efficiently between blocks while offering deterministic latency, congestion management, and quality-of-service guarantees.

Traditional bus-based architectures (such as AMBA AXI) work adequately for simple SoCs with limited masters and slaves, but encounter fundamental scalability constraints beyond 10–20 functional blocks: bandwidth contention, routing congestion, and verification complexity all increase non-linearly. NoC architectures solve this through mesh or ring topologies that scale gracefully with design complexity. We characterise NoC as a strategic asset rather than commodity: as transistor scaling slows, architectural efficiency drives performance, making sophisticated NoC IP critical for AI accelerators, multi-die chips, HPC, chipllets, and edge AI SoCs.

The commercial NoC IP landscape has consolidated significantly. In 2018, Intel acquired the NetSpeed team, removing one of only three commercial NoC IP providers from the open market. In 2019, Facebook (now Meta) acquired Sonics, though Sonics had already pivoted from NoC to energy/power management IP in 2016, so it had effectively exited the commercial NoC market before acquisition. Following these moves, Arteris IP (NASDAQ: AIP) is widely recognised as the only remaining licensable commercial NoC IP supplier, a position Arteris itself confirmed publicly: "we are the only licensable-NoC supplier." (Source: Semiwiki) SkyeChip's proprietary in-house NoC IP therefore competes in an extremely concentrated market where the primary commercial alternative is Arteris, a listed US company with FY2025 total revenue of USD70.58m (encompassing both NoC System IP and SoC Integration Automation software).

Demand for NoC IP is accelerating for three structural reasons. First, chipllet-based architectures require sophisticated communication across multiple dies - NoC IP is a critical enabler of this integration. Second, AI accelerator SoCs are among the most complex chips ever designed, requiring NoC to orchestrate data flow across 50+ functional blocks. Third, the UCle standard is driving convergence between on-chip interconnect (NoC) and inter-chip interconnect (D2D), creating a natural adjacency for providers like SkyeChip that offer both.

“Our View: SkyeChip's NoC IP accounted for **c.16%** of FPE Oct 2025 total revenue (RM14.3m), the only period for which a sub-segment breakdown has been publicly disclosed. No equivalent FY25 or FY26 full-year breakdown has been published. For FY26, total silicon IP revenue grew **c.39.3%** to RM119.4m, implying NoC IP contributed an estimated RM19m+ on the same proportional basis, though no sub-segment breakdown has been published for FY26. The Group's NoC IP is complemented by the in-house RAPTuner EDA tool, a proprietary network architecture simulation and optimisation tool currently bundled with NoC IP offerings at no additional charge, with longer-term standalone monetisation potential.

Die-to-Die (D2D) Interface IP - The Chiplet Glue

Die-to-die interface IP enables high-speed communication between separate silicon dies (chiplets) within a single semiconductor package. According to SNS Insider, the global die-to-die IP market was valued at **USD1.80bn in 2025 and is projected to reach USD3.72bn by 2033 at a CAGR of 9.57%**. UCle (Universal Chiplet Interconnect Express) dominated with 53.4% share in 2025, and HPC/AI accelerators accounted for 41.9% of D2D IP demand.

The chiplet interconnect market more broadly: encompassing the packaging, interposers, and interface IP required for multi-die integration, was valued at **USD2.17bn in 2025 and is projected to grow at a CAGR of 34.4% to USD41.2bn by 2035**, according to Global Market Insights. R&D investment in this space is accelerating rapidly: patent filings in the chiplet interconnect domain grew from 152 in 2017 to 1,070 in 2024, a seven-fold increase - with the 2022–2024 period alone accounting for 55% of all historical filings. (PATsnap)

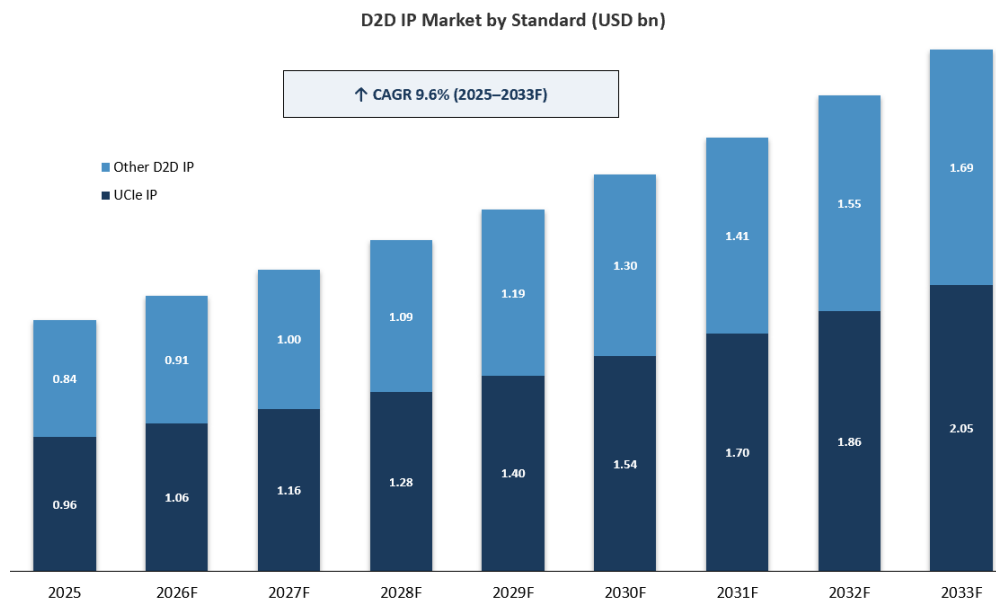
The UCle consortium has grown to 120+ members as of 2026, including Intel, AMD, TSMC, Samsung, Arm, Meta, and Google - establishing UCle as the de facto open standard for die-to-die chiplet communication. UCle version history: (Source: PatSnap)

- (i) **UCle 1.0 (March 2022):** 16 Gbps PHY speeds; first open standardised die-to-die interconnect specification (UCIE)
- (ii) **UCle 1.1 (August 2023):** Up to 16 Gbps for standard packaging and up to 32 Gbps for advanced packaging (CoWoS, EMIB); added multi-protocol link tunneling for 2D and 2.5D packaging optimisation. (UCIE)
- (iii) **UCle 2.0 (August 2024):** Maximum data rates unchanged at 16/32 Gbps (standard/advanced packaging); primary focus was standardised system architecture for 3D vertical packaging integration and the introduction of UCle DFX Architecture (UDA) for testing, manageability, and debugging throughout the chiplet lifecycle. (UCIE)

A future version targeting 64 Gbps speeds and optical die-to-die options is anticipated in 2026–2027, though no official UCle version number has been confirmed by the consortium. Proprietary die-to-die links outside single-vendor ecosystems are becoming increasingly obsolete as UCle reaches critical mass across the industry. (PatSnap,UCIE)

Our View. The proliferation of chiplets creates compounding demand for interface IP providers for four structural reasons: (i) more design starts require more interface IP licences; (ii) each chiplet integration requires UCle D2D interface IP; (iii) IP must be validated across multiple foundry PDKs; and (iv) each node migration triggers IP re-qualification. Together these create a structural multiplier effect on interface IP demand as the chiplet era matures. SkyeChip's UCle-compliant D2D interface IP accounted for an estimated 4.7% of FPE Oct 2025 total revenue (RM4.2m), the only period for which a sub-segment breakdown has been publicly disclosed. No equivalent FY25 or FY26 full-year breakdown has been published. For FY26, total silicon IP revenue grew 39.3% to RM119.4m; assuming D2D IP grew broadly in line with total revenue (+29.7%), D2D would have contributed an estimated RM5–6m, though this is our own estimate and the actual figure may differ depending on the relative growth rate of D2D engagements versus other silicon IP categories.

Figure 24: D2D IP Market by Standard (USD bn)



Source: SNSInsider, Apex Securities

Process Node Migration - 3nm, 2nm, and Beyond

The semiconductor industry's relentless push to smaller process nodes creates both challenges and opportunities for IP providers. Each new node requires IP blocks to be redesigned, re-characterised, and re-validated - a process costing tens of millions of dollars per IP block. **This re-qualification cycle is fundamental to the silicon IP business model, creating natural re-licensing triggers as customers migrate across generations.**

3nm is in volume production at TSMC (N3, N3E, N3P) and Samsung (3GAE, 3GAP). SkyeChip has access to PDKs from foundries enabling IC and silicon IP design down to 3nm process nodes and its HBM3E interface IP has been silicon-proven at 4nm (8,800 Mbps first-time success), placing it among a select group of IP providers with validated advanced-node capability.

2nm is now in early volume production. TSMC's N2 node entered volume production in H2 2025, while Intel's 18A is ramping through 2026 for its Core Series 3 and Xeon 6+ processors, with the upgraded 18A-P node entering initial production as announced at Computex 2026. Google has placed orders for Intel to build chips on its advanced nodes, while NVIDIA is testing Intel's processes for potential future use (The Information), validating Intel Foundry as a credible alternative to TSMC. These nodes introduce gate-all-around (GAA) transistor architecture, the most significant transistor design change since FinFET at 22nm, and every IP block must be redesigned for GAA, creating a major re-licensing wave. SkyeChip has allocated RM56.4m of IPO proceeds for silicon IP R&D targeting 2nm process nodes and joined the Intel Foundry Accelerator IP Alliance in January 2025, providing access to Intel's 18A and 18A-P process technologies and expanding the potential customer base for SkyeChip's interface IP across a second major foundry ecosystem

Sub-2nm is no longer a distant research concept: it is an actively resourced production programme. TSMC unveiled its A14 (1.4nm-class) process technology at its North America Technology Symposium on 23 April 2025, based on 2nd Generation gate-all-around (GAA) nanosheet transistors and its NanoFlex Pro standard cell architecture. Compared to N2 (2nm), A14 delivers up to 15% higher performance at the same power, or up to 30% lower power at the same speed, with over 20% improvement in logic density. **Crucially, TSMC confirmed that A14 yield performance is ahead of schedule, with risk production targeted for 2027 and mass production for H2 2028.** TSMC has also broken ground on Fab 25 (Central Taiwan Science Park), a NT\$1.5 trillion (USD49bn) facility dedicated to A14. Beyond A14, TSMC has already announced A13 (optical shrink of A14) and A12 (with backside power delivery, targeting HPC/AI) for 2029.

Since A14 is an all-new node with new GAA standard cells, it requires entirely new IP blocks - it is not compatible with N2 or N2P IP, creating a full re-licensing wave. IP development for A14 must begin 18–36 months before production, meaning IP providers need A14-ready portfolios by early 2028 at the latest. SkyeChip's IPO-funded R&D programme, including its Intel Foundry Accelerator IP Alliance membership giving access to Intel's 18A and 14A nodes. ***This positions the Group to participate in this next-generation IP development cycle across both TSMC and Intel foundry ecosystems. (Source:TSMC, Tom's Hardware)***

“Our View: The node migration dynamic structurally favours established IP providers over newcomers: each transition creates a re-licensing event for existing customers while simultaneously raising the barrier to entry for new competitors who must qualify IP at each successive node.”

The RISC-V Opportunity

RISC-V, the open-source instruction set architecture, has reached a watershed moment: c.25% of the global processor market as of January 2026, marking the end of the long-standing x86 and Arm duopoly. (Financial Content)

The RISC-V technology market is projected to grow from **c.USD1.3–2.5bn** in 2025 to **c.USD8.6–10.8bn** by 2030–2031, at a CAGR of 30–42% depending on research firm methodology reflecting genuine divergence in scope definitions across providers. (Source: Mordor Intelligence, March 2026: USD1.34bn to USD10.62bn 2031 at 41.23% CAGR; GMI: USD2.30bn to USD8.57bn 2030 at 30.7%; NextMSC: USD2.20bn to USD9.08bn 2030 at 32.8%)

Growth is driven by: (i) the cost advantage of royalty-free architectures versus Arm's licensing fees; (ii) government-backed semiconductor sovereignty programmes in China, the EU, India, and Saudi Arabia; (iii) rapid adoption in cloud AI accelerators and edge computing; and (iv) a maturing software ecosystem, with the RISC-V Software Ecosystem (RISE) project, supported by Alphabet, ensuring Android and major Linux distributions now offer RISC-V support. IoT devices held 34.5% of RISC-V revenue share in 2025, with data centres recording the fastest growth at 42.6% CAGR as hyperscalers integrate open-ISA inference tiles to reduce power draw and total cost of ownership. (Source: Mordor Intelligence)

Chinese players are advancing rapidly. Nuclei System Technology and StarFive are gaining traction through government-supported initiatives. StarFive received investment from HKIC to expand RISC-V chip applications.

Our View. SkyeChip's RISC-V SoC contract (September 2025) positions the Group within this high-growth architecture. While the initial contract represents a single ASIC engagement, the strategic value lies in developing RISC-V design capabilities applicable across future customers, particularly Chinese chip designers for whom RISC-V offers architectural independence from both Arm and x86. The prospectus confirms the Group has earmarked a portion of its R&D budget for RISC-V SoC development as part of its product expansion roadmap.

Figure 25: Research Provider Estimates - RISC-V Market Size & CAGR

Research Firm	2025 Base (USD bn)	Forecast Year	Projected Size	CAGR
Mordor Intelligence	USD 1.34bn	2031	USD 10.62bn	41.23%
Global Market Insights	USD 2.30bn	2030	USD 8.57bn	30.7%
NextMSC	USD 2.20bn	2030	USD 9.08bn	32.8%

Source: Various, Apex Securities

The Chinese AI Chip Ecosystem - SkyeChip's Primary Market

For a detailed discussion of US export controls and their implications for SkyeChip, refer to Investment Thesis #3 and Investment Risk: Geographic Concentration.

The key structural dynamic is that US export restrictions have forced Chinese AI companies to design indigenous alternatives to NVIDIA/AMD chips, creating massive demand for third-party IP from non-US suppliers. China has committed an estimated **c.USD200bn** in aggregate semiconductor support over the next five years - combining Big Fund III (RMB344bn / c.USD47bn announced in 2024), provincial and local semiconductor investment funds, R&D tax credit programmes (up to 220% deduction for semiconductor chip R&D), and additional incentive packages under deliberation (Semianalysis). China has already channelled an estimated **USD142-150bn** into its semiconductor industry historically between 2014 and 2023, **3.6x higher than the US within the same period**. (Tom's Hardware)

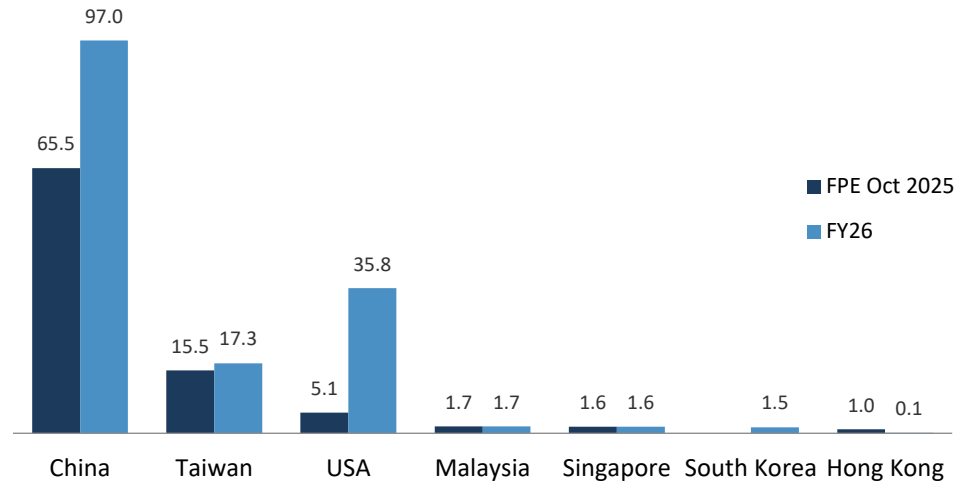
CXMT, China's DRAM national champion, has accelerated its HBM development well ahead of original projections - beginning HBM2 (4-layer) mass production in H2 2024 (two years ahead of the previously expected 2026 target) according to Tom's Hardware, supplying HBM3 samples to Huawei and other domestic AI chip designers from H2 2025, and targeting HBM3 mass production in 2026 and HBM3E by 2027 (chinatalk). CXMT is converting approximately **20% of its total DRAM capacity - c.60,000 wafers per month** to HBM production and is building a new Shanghai fab two to three times the size of its existing Hefei headquarters. In parallel, Huawei has established its own HBM supply chain with XMC (Wuhan Xinxin) producing HBM wafers and SJSemi (Shenghe Jingwei Semiconductor) handling packaging (Tom's Hardware). China and Taiwan together accounted for 73.8% of SkyeChip's FY26 revenue (China: 62.6% / RM97.0m, Taiwan: 11.2% / RM17.3m) which is a meaningful improvement from 90.6% in FPE Oct 2025, driven by the emergence of US revenue at 23.1% (RM35.8m) and South Korea as a new market at c.1.0% (RM1.5m).

Our View. China is not merely SkyeChip's largest market, it is the structural reason SkyeChip exists as an independent IP company with a differentiated competitive position. The confluence of US export controls on advanced AI chips, US export controls on EDA tools, and the Chinese government's **USD200bn+** semiconductor support programme has created a captive, growing, and structurally loyal demand base for exactly the IP that SkyeChip provides. Chinese AI chip designers, unable to purchase NVIDIA GPUs and increasingly cautious about relying on US-domiciled IP vendors - require HBM interface IP, NoC IP, and D2D interconnect IP from providers outside the US export control jurisdiction. **SkyeChip, as a Malaysian-incorporated company with no US-origin technology restrictions, sits in precisely this gap.**

The risk, however, is concentration: at **62.6%** of FY26 revenue, any deterioration in the Chinese AI chip design ecosystem, whether from domestic policy shifts, sanctions escalation targeting Malaysian intermediaries, or a slowdown in AI capex, would materially impact earnings. The FY26 trajectory is therefore encouraging on two fronts simultaneously: China revenue grew in absolute terms (RM97.0m in FY26 vs RM67.5m in FY25, +43.8% YoY) even as its share of total revenue improved materially from **73.3%** (FPE Oct 2025) to **62.6%**, meaning the China business is growing strongly while the Group simultaneously diversifies. CXMT's acceleration, with its HBM2 mass production two years ahead of schedule, HBM3 samples in H2 2025, HBM3 mass production targeted in 2026 and HBM3E in 2027, is a direct demand signal for SkyeChip's HBM interface IP portfolio: every new generation of Chinese HBM requires a new generation of interface IP, and the qualification cycle means customers need to engage IP providers 18-36 months before mass production targets. The Huawei-XMC-SJSemi HBM supply chain development further confirms that China's HBM ecosystem is building out at every layer of the stack and SkyeChip's Malaysian domicile means it can participate in this supply chain without the geopolitical friction that would attach to a US or Taiwanese IP provider.

We view China as a structurally durable market for SkyeChip over the medium term, with the key risk being the pace at which the Group can continue diversifying its revenue base a process that, based on FY26 data, is already underway at impressive speed.

Figure 26: SkyeChip Geographic Revenue - Diversification from FPE Oct 2025 to FY26



Source: Company, Apex Securities

The US Market - SkyeChip's Fastest-Growing Geography

The United States has emerged as SkyeChip's most significant geographic growth story. **US revenue surged from 5.7% of FPE Oct 2025 revenue to 23.1% (RM35.8m) of FY26 revenue, with Q4 FY26 alone contributing RM28.9m - 49% of quarterly revenue.**

The US custom ASIC and AI chip design ecosystem is the largest globally. According to TrendForce, custom ASIC shipments from cloud providers are projected to grow **44.6%** in 2026, versus **16.1%** for GPU shipments, signalling a structural shift in the AI hardware landscape. The CHIPS and Science Act is reshaping the US semiconductor landscape. The **USD52.7bn** federal programme, comprising USD39bn in manufacturing incentives, USD11bn for R&D, and a 25% tax credit for manufacturing equipment (Norton Rose), has mobilised over **USD630bn** in announced private sector investments across more than **140 projects in 28 states** (SIA), creating an estimated **500,000 jobs**. The National Semiconductor Technology Center (NSTC) is also establishing design enablement gateways, silicon aggregation services, and venture funds enabling startups to access leading-edge nodes previously reserved for large incumbents.

The US AI chip startup ecosystem is a direct demand driver for SkyeChip. Global investments in AI chip hardware startups reached over USD11.6bn in 2025, with Tenstorrent, Cerebras, Enflame, and other inference accelerator and custom ASIC platform companies among the largest recipients - up significantly from prior years. (electroiq.com) Semiconductor Engineering's quarterly tracker recorded **80 startups raising USD8.4bn in Q3 2025 alone, followed by 75 startups raising USD3bn in Q4 2025**. As of April 2026, the trailing 12-month AI chip funding market totals approximately **USD8.0bn** across **19 disclosed deals**, heavily concentrated in inference accelerators (47.4% of deal count) and data centre compute (46.1% of capital) the precise customer segments that require SkyeChip's memory interface and NoC IP (New Market Pitch). The market is characterised by power-law concentration: the top 10 deals account for **c.82.4%** of disclosed capital, confirming that investment is flowing at manufacturing and deployment scale, not early-stage validation. For broader context, total global VC investment in AI companies reached **c.USD211-259bn in 2025** (+85% YoY), with AI capturing over **c.50-61%** of all global VC deal value for the first time in history (Crunchbase). While this broader figure encompasses foundation model companies and AI applications, it underscores the structural acceleration in AI-related capital deployment that ultimately drives custom chip design activity.

These startups typically lack internal silicon design teams and focus on their core AI algorithm competencies, licensing available IP designs to accelerate development and time to market. **This creates structural demand for memory interface, NoC, and D2D IP from specialist providers like SkyeChip.**

Our View and Strategic Implications. SkyeChip's Malaysian domicile is a structural advantage in the US market, as a geopolitically neutral, non-Chinese vendor, it avoids the sensitivities that can complicate Chinese IP vendors' engagement with US customers, while simultaneously remaining unconstrained by CHIPS Act restrictions that limit US-funded recipients from expanding in China, a dual positioning that very few IP providers can credibly claim in today's bifurcated semiconductor landscape. The Intel Foundry Accelerator IP Alliance membership which the company joined in January 2025 is a potentially significant US market catalyst: Intel Foundry is aggressively rebuilding its external customer ecosystem for its 18A and 14A nodes targeting AI and HPC applications, and by having formal access to Intel Foundry's process technologies, SkyeChip gains early PDK access, technical collaboration, and visibility within Intel Foundry's own IP ecosystem, increasing the probability of being introduced to US-based fabless customers evaluating Intel Foundry as a manufacturing partner, creating a structural referral channel that does not require a US sales office to activate. The Group also plans to establish a US sales and R&D office within the **RM19.0m operational facilities budget**, and the speed of US revenue growth from negligible to **23.1% of Group revenue (RM35.8m)** in FY26, with Q4 FY26 US revenue of RM28.9m representing **49%** of quarterly revenue, suggests the addressable market opportunity is substantial and initial customer wins are translating into broader adoption at pace.

Figure 27: CHIPS and Science Act - Funding Structure & Market Impact

Programme Component	Federal Allocation	% of Total	Key Mechanism	Source
Manufacturing Incentives (CHIPS Program Office)	USD 39.0bn	74.0%	<i>Grants, loans and loan guarantees for semiconductor fabs</i>	<i>Norton Rose Fulbright, Nov 2024</i>
R&D (CHIPS R&D Office / NSTC)	USD 11.0bn	20.9%	<i>NSTC design enablement, silicon aggregation, workforce</i>	<i>Norton Rose Fulbright, Nov 2024</i>
Mature Semiconductor Manufacturing	USD 2.0bn	3.8%	<i>Military, automotive, and manufacturing-grade chips</i>	<i>McKinsey, 2025</i>
25% Manufacturing Tax Credit	~USD 0.7bn est.	1.3%	<i>Investment tax credit on semiconductor equipment purchases</i>	<i>Vyrian, Jan 2026; McKinsey</i>
Total CHIPS Programme	USD 52.7bn	100%		

Source: Norton Rose Fullbright, Mckinsey, Apex Securities

Vietnam - Emerging Semiconductor Hub and SkyeChip's Operational Base

Vietnam is rapidly transitioning from a back-end assembly, test, and packaging (ATP) hub towards front-end IC design and wafer fabrication. Capitalising on this, SkyeChip has established operational presence through SkyeChip Solutions Vietnam Co Ltd, which commenced operations in December 2024 and benefits from a 5-year corporate income tax exemption commencing May 2025 which is a meaningful structural cost advantage relative to its Malaysia-only operations. Management has guided that Vietnam is expected to contribute approximately **c.12–17%** of Group revenue over the medium term, reflecting both its role as a cost-competitive engineering base and its growing importance as a potential customer market.

Policy commitment. The Vietnamese government has designated semiconductors as a strategic national priority under Strategy 1018 (Decision 1018/QD-TTg, signed 21 September 2024, development of Vietnam's semiconductor industry through 2030, with a vision to 2050) and Programme 1017 (human resources development for the sector). The Law on Digital Technology Industry effective 1 January 2026, is one of the first standalone legislative frameworks of its kind, creating a comprehensive legal foundation for semiconductor development including corporate income tax incentives, cost subsidies, customs facilitation, and human capital programmes (Source: Vietnam Briefing, January 2026). As of March 2026, Vietnam had secured **241** foreign-invested semiconductor projects with total registered capital of **USD14.2bn up from 174**

projects / USD11.6bn as at December 2024, confirmed by the National Steering Committee for Semiconductor Industry Development (TechNode Global). **The jump from 174 projects / USD11.6bn (December 2024) to 241 projects / USD14.2bn (March 2026)** in just 15 months reflects the rapid acceleration of semiconductor FDI into Vietnam, **adding 67 new projects and USD2.6bn** in registered capital in roughly one year.

Vietnam semiconductor market sizing. The Vietnam semiconductor market was valued at USD7.03bn in 2024 and is projected to reach **USD16.64bn by 2033 at a CAGR of 9.30%** (IMARC Group). Mordor Intelligence however, estimates the 2025 market at USD10.16bn, growing to **USD16.51bn by 2030 at a 10.23% CAGR**, reflecting the broader scope of Vietnam's semiconductor ecosystem including assembly, test, and packaging activity (Mordor Intelligence). SEMI projects the Vietnam semiconductor market to reach **USD31.28bn by 2027**, growing at **11.6% CAGR from 2023 to 2027**, the highest projection, likely including Samsung's large electronics manufacturing revenue base. Technavio's updated 2026-2030 forecast projects Vietnam's semiconductor market to grow by approximately **USD2.2bn at a 7.1% CAGR between 2025 and 2030**, driven by rising high-tech FDI and supply chain diversification from China (Technavio). The wide divergence across research firms reflects genuinely different scope definitions, narrower figures (IMARC) cover semiconductor components only, while broader figures (SEMI) include Samsung's Vietnam electronics manufacturing revenue.

Workforce Scaling. Vietnam currently has approximately **7,000 chip design engineers** across 50 semiconductor design businesses, with 166 universities offering semiconductor-related courses enrolling 134,000 students annually (TechNode Global). The government targets 50,000 semiconductor engineers by 2030 (including 15,000 IC design specialists) and 100,000+ by 2040 under Strategy 1018 (SEMI). Three high-tech zones in Hanoi, Ho Chi Minh City, and Da Nang serve as anchor hubs. Global players have established or expanded R&D operations, including Intel (Intel Products Vietnam in HCMC, the company's largest back-end facility worldwide with over 3.9 billion units shipped), Qualcomm (first R&D centre in Southeast Asia, Hanoi), NVIDIA (two AI centres being established under the December 2024 Government-NVIDIA agreement), Cadence, and Keysight (Source: Delco Construction).

Two Samsung entities represent the most significant recent investment announcements and are directly relevant to SkyeChip's opportunity:

- (i) **Samsung Electro-Mechanics (SEMCO) is investing approximately USD1.2bn (c.KRW1.8 trillion) to build a new large-scale flip-chip ball grid array (FC-BGA) factory in Vietnam, a high-density package substrate critical for AI semiconductor packaging.** With this investment, SEMCO's cumulative FC-BGA production facilities in Vietnam will reach approximately KRW3 trillion (c.USD2.2bn). SEMCO has secured contracts to supply FC-BGA substrates for AI semiconductors, with its customer base expanding to include Groq (for its Language Processing Unit), Broadcom, Google, Amazon, and Apple, all of whom are developing custom AI chips that require advanced FC-BGA substrates. The proliferation of FC-BGA-based advanced packaging drives demand for memory interface and die-to-die interconnect IP that enables heterogeneous chip integration on these substrates, directly adjacent to SkyeChip's IP portfolio. (Seoul Economic Daily)
- (ii) **Samsung Electronics is considering a further phased investment of approximately USD4bn in chip testing and packaging facilities in northern Vietnam (Thai Nguyen province, already a Samsung production base with USD4.4bn in new investment commitments secured at the start of 2026).** Vietnam's Ministry of Finance confirmed it is coordinating with other ministries to finalise and submit to the Prime Minister a Memorandum of Understanding between the Government of Vietnam and Samsung Group regarding the semiconductor manufacturing project. **Samsung is already the largest single foreign investor in Vietnam with over USD23bn invested across six manufacturing plants and one**

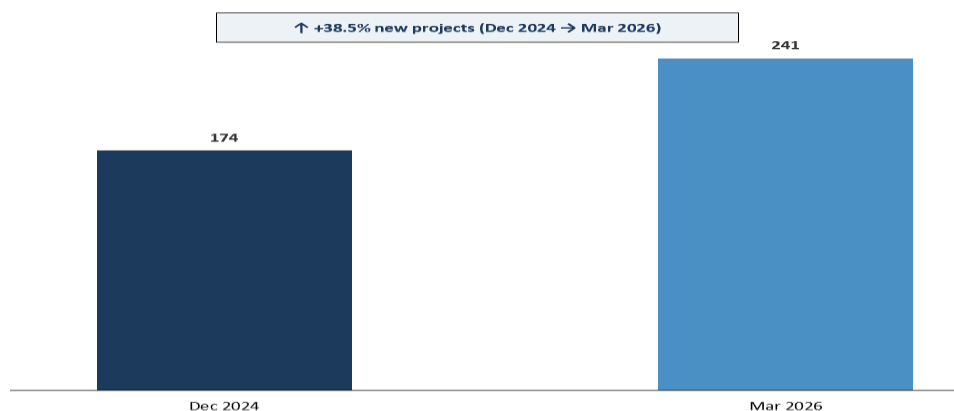
R&D centre (Reuters). The convergence of Samsung SEMCO's FC-BGA expansion and Samsung Electronics' planned testing/packaging investment confirms Vietnam's transition from ATP workhorse to advanced packaging hub - a structural upgrade that will require increasingly sophisticated interface IP for heterogeneous chip integration. **This is SkyeChip's addressable market within the Vietnamese semiconductor ecosystem over the medium term.**

Moving beyond ATP. Viettel Group, Vietnam's state-owned telecommunications conglomerate broke ground on the country's first semiconductor chip fabrication plant in January 2026 at Hoa Lac Hi-Tech Park in Hanoi, targeting trial production of 32nm chips by end-2027 (TechNode Global). The National Centre for Semiconductor Chip Design, established in December 2025, provides infrastructure for chip prototyping, connecting research institutions and design companies with fabrication and packaging facilities (Source: Vietnam Briefing). Vietnam currently has 50 semiconductor design businesses, with FPT Semiconductor designing ICs for IoT, automotive, and consumer electronics, and NVIDIA-FPT signing an AI chip partnership (Source: TechNode Global). Prime Minister Pham Minh Chinh reiterated a target of self-reliance in semiconductor design, manufacturing, and testing by 2027 at a national committee meeting on 4 August 2025 (Source: SEMI).

Our View and Strategic implications for SkyeChip. Vietnam presents a dual opportunity, as both an operational base and an emerging customer market that is becoming more compelling with each passing quarter. On the operational side, SkyeChip's Vietnam subsidiary (SkyeChip Solutions Vietnam Co Ltd, operational since December 2024) provides cost-competitive engineering capacity with a five-year corporate income tax exemption commencing May 2025, with VNCHIP Technology Joint Stock Company already providing outsourced IC design services to the Group accounting for **c.8.2%** of operational costs in FPEOct 2025 and R&D office expansion in both Malaysia and Vietnam planned for 2026–2029 within the RM19.0m operational facilities budget.

Vietnam's semiconductor FDI surged from **174 projects / USD11.6bn** (December 2024) to **241 projects / USD14.2bn** (March 2026) in just **15 months** (TechNode Global, 31 March 2026), anchored by Samsung Electronics (USD23bn cumulative investment, USD4bn chip testing and packaging facility under MOU negotiation), Samsung Electro-Mechanics (USD1.2bn FC-BGA factory for AI chip substrates, supplying high-density package substrates for AI semiconductors to customers including Groq for its Language Processing Unit and FC-BGA substrates for custom AI chips designed by Broadcom, Google, Amazon, and Apple), Intel, Qualcomm, and NVIDIA. This creates a rapidly expanding talent pool and engineering ecosystem for SkyeChip to draw upon. On the customer side, as Vietnamese IC design companies mature, with the government targeting **100 design companies by 2030 up from 50 currently**, they will increasingly require licensed IP blocks for memory interfaces, NoC, and D2D interconnect, and Samsung SEMCO's FC-BGA and advanced packaging build-out specifically requires sophisticated interface IP for heterogeneous chip integration, precisely SkyeChip's addressable market. Management is guiding for Vietnam to contribute **c.12-17%** of Group revenue over the medium term and the Vietnam semiconductor market is forecast to grow **at 9-10% CAGR through 2033**. Hence, we view Vietnam as a meaningful and rapidly maturing contributor to SkyeChip's geographic diversification strategy beyond China.

Figure 28: Vietnam Semiconductor FDI Projects



Source: Technode Global,, Apex Securities

Figure 29: Vietnam Semiconductor Market

Research Firm	Base Year / Size	Forecast Year	Projected Size	CAGR
IMARC Group	USD7.03bn (2024)	2033	USD16.64bn	9.30%
Mordor Intelligence	USD10.16bn (2025)	2030	USD16.51bn	10.23%
Technavio	USD2.2bn growth (2025–30)	2030	Base+USD2.2bn	7.1%
SEMI	~USD10–12bn (2023)	2027	USD31.28bn	11.6%

Source: Various, Apex Securities

Figure 30: Vietnam Semiconductor Workforce Scaling - Current State vs 2030 Target

Metric	Current (2025/26)	2030 Target	2040 Target	Gap to 2030	Source
Total semiconductor engineers	~7,000	50,000	100,000+	+43,000	Strategy 1018; SEMI; Technode
IC design specialists	~4,000–5,000	15,000	n/a	+10,000–11,000	Strategy 1018; SEMI Sep 2025
Semiconductor design companies	50	100	300+	+50	Strategy 1018; Technode Mar 2026
Universities offering courses	166	n/a	n/a	Growing	Technode Global, Mar 2026
Annual student enrollment	134,000	n/a	n/a	Growing	Technode Global, Mar 2026
FDI semiconductor projects	241 (Mar 2026)	n/a	n/a	Growing	Technode Global, Mar 2026

Source: SEMI, Technode Global, Apex Securities

South Korea - Emerging Optionality from the "K-Nvidia" AI Chip Ecosystem

South Korea emerged as a new market for SkyeChip in FY26, contributing **c.1.0% (c.RM1.5m)** of Group revenue, booked entirely in Q4 FY26. While small in absolute terms, South Korea represents a potentially significant growth vector given the country's massive semiconductor ecosystem and its aggressive government-backed push into AI chip design.

South Korea is a global semiconductor powerhouse but has a critical gap in IC design: despite global dominance in memory chips through Samsung and SK Hynix, Korea's IC design market share stands at approximately **2%** globally, according to the Korea Fabless Industry Association (KFIA) creating a structural opening. The country has world-class foundry capacity (Samsung Foundry), world-class memory technology, and is now deploying unprecedented capital to build a domestic AI chip design ecosystem.

The "K-Nvidia" initiative is channelling unprecedented capital into Korean AI chip startups. In March 2026, South Korea's Ministry of Science and ICT and the Financial Services Commission jointly unveiled the K-Nvidia initiative, backed by a **150 trillion won (c.USD100bn)** National Growth Fund to be created over five years, of which approximately **51 trillion won (c.USD34bn)** is allocated specifically to AI (30 trillion won) and semiconductors (21 trillion won) according to UPI. The government plans to deploy over 30 trillion won across all sectors in 2026 alone, including 6 trillion won for AI and 4.2 trillion won for semiconductor, totalling approximately 10.2 trillion won in AI+semiconductor investment in 2026 alone (The Legal Wire). The fund is structured as a direct equity investment vehicle, taking stakes in designated national champions; the first investment was **KRW250bn (c.USD170m)** directly into Rebellions, marking the first state equity commitment under the K-Nvidia Initiative. (AOL, Seoul Economic Daily)

Five domestic NPU developers have been designated as eligible K-Nvidia candidates: Rebellions, FuriosaAI, DeepX, HyperAccel, and Mobilint - with the first three absorbing nearly all the capital. Together, Rebellions, FuriosaAI, and DeepX have raised over USD1.5bn in combined funding. (Seoulz)

- (i) **Rebellions:** Most recent pre-IPO round raised KRW640bn at a valuation of KRW3.4 trillion (c.USD2.3bn), with total funding of USD850m. The National Growth Fund made its first direct equity investment here (KRW250bn / c.USD178m). Rebellions is targeting a KOSPI IPO in Q32026 with JPMorgan as global lead underwriter. Its Rebel100 chip uses a chiplet architecture with four compute dies manufactured by Samsung, UClc interconnects, and 144GB of HBM3E memory, which is directly the pain point SkyeChip is targeting: UClc-compliant D2D interface IP and HBM3E memory interface IP. (Source: Seoul Economic Daily)
- (ii) **FuriosaAI:** Began mass production of its 5nm RNGD inference chip in January 2026, with HBM3E-upgraded variants (Renegade+ and Renegade+ Max targeting 144GB single-card memory) in development. FuriosaAI demonstrated its RNGD running OpenAI's gpt-oss 120B model in September 2025. Current valuation: KRW3 trillion (as of May 2026 pre-IPO round of KRW750bn). A Nasdaq or KRX listing is under consideration. (Source: Seoul Economic Daily, Seoulz)
- (iii) **DeepX:** Edge AI NPU designer founded by former Apple A11 Bionic designer Lokwon Kim; valuation approaching KRW800bn (near unicorn status); doubled workforce from 70 to 140+ in 2025 alone. (Source: Seoulz)

These AI chip startups are precisely the customer profile that SkyeChip serves Rebellions' Rebel100 uses HBM3E + UClc + chiplet architecture, all three requiring SkyeChip's IP stack. FuriosaAI's RNGD and HBM3E variants require validated HBM3E memory interface IP. As these companies scale from prototype to mass production with Rebellions targeting 4nm next generation and FuriosaAI at 5nm, their IP requirements intensify and the switching cost of changing IP vendors increases. (TheAIWorld, Seoulz).

Our View and Strategic Implications. South Korea represents upside to our base case forecast, though we have included a modest Korea revenue contribution in our FY27F+ estimates given the commercial traction established in Q4 FY26, and is best characterised as an optionality play on a government-backed AI chip ecosystem being built from scratch with **c.USD33bn+** in committed capital, where SkyeChip has already established a direct commercial channel before most investors have noticed. SkyeChip's UClc-Advanced Package 32G PHY IP was listed on Samsung Foundry CONNECT on 16 February 2026, Samsung Foundry's IP ecosystem platform, implemented on Samsung SF4X (4nm) and supporting 32GT/s UClc Advanced Package applications. This enables Samsung Foundry customers to directly discover, evaluate, and engage with SkyeChip as part of Samsung's chiplet ecosystem without requiring a Korea sales office to activate. The timing is striking: the Samsung CONNECT listing (16 February 2026) falls within Q4 FY26 (January-March 2026), the same quarter SkyeChip first recorded **c.RM1.5m** of South Korea revenue, consistent with the listing generating its first Korean customer engagement shortly after going live.

The technical case is compelling: Rebellions' Rebel100 uses UCIe interconnects and 144GB HBM3E, and FuriosaAI's RINGD and planned HBM3E-upgraded variants (Renegade+, Renegade+Max) similarly require validated HBM3E interface IP, both directly within SkyeChip's IP portfolio, and both companies are K-Nvidia designated champions with **USD850m+** (Rebellions) and **KRW750bn** (FuriosaAI) in pre-IPO funding respectively, giving them the capital to pay for best-in-class IP. SkyeChip's geopolitical neutrality as a Malaysian company further advantages it over US-headquartered incumbents (Synopsys, Cadence, Rambus) as Korean chip designers de-risk their IP supply chains. If Korea follows even a fraction of the US trajectory, which went from negligible to **23.1%** of Group revenue in FY26, the revenue contribution could be material within two to three years, and the Samsung CONNECT platform puts SkyeChip in the discovery path of every Samsung Foundry customer in Korea at zero incremental cost.

Data Centres and the AI Capex Supercycle

For a detailed discussion of hyperscaler capex and its implications for semiconductor IP demand, refer to **Investment Thesis #3: Riding the AI Chip Supercycle**.

The AI infrastructure buildout is the largest capital expenditure programme in technology history, and SkyeChip is positioned to benefit from every dollar spent. In 2026, the four largest hyperscalers (Amazon, Google, Meta, and Microsoft) have collectively committed to spending c.USD725bn on capital expenditure, nearly doubling the record **c.USD410bn** spent in 2025. (Source: Financial Times, May 2026; Tom's Hardware) Including Oracle, total Big Five hyperscaler capex is approaching **c.USD775bn**. (Source: Futurum Group). The vast majority of this spending, estimated at **c.75%**, or **USD540-550bn+**, is directed at AI infrastructure: GPUs, custom AI accelerators, servers, networking, and data centres (Source: CreditSights). Q1 2026 alone saw the Big Four spend **USD130bn combined, 3.7x the USD35bn they spent in Q1 2023**, confirming the trajectory is accelerating, not moderating. (Source: businessengineer.ai)

Every AI chip at the heart of these data centres requires memory interfaces and on-chip interconnects. A single NVIDIA Blackwell Ultra GPU uses up to 288 GB of HBM3E, with each HBM stack connected to the processor through an interface that must be designed, verified, and silicon-proven. Custom AI accelerators being developed by the hyperscalers themselves, Amazon's Trainium, Google's TPU, Microsoft's Maia, all face the same requirement, Google (TPU v7-v9p with Broadcom/MediaTek), Amazon (Trainium 2-4 with Marvell/Alchip), Microsoft (Maia 200-300 with GUC/Marvell), Meta (MTIA 300-600 with Broadcom), Apple (Baltra-Sotra with Broadcom), xAI (X1 with Broadcom), and SoftBank (Izanagi with Broadcom). **Every one of these interfaces represents a potential licensing opportunity for companies like SkyeChip.**

The Broadcom parallel is directly instructive for understanding SkyeChip's strategic trajectory. Broadcom, under Hock Tan, built deep IP expertise in high-speed SerDes interconnect which is essential for connecting thousands of AI cores together at scale and leveraged this into winning custom AI ASIC contracts for Google (TPU), Meta, ByteDance, and OpenAI, delivering finished silicon at gross margins north of **c.65%**. SkyeChip is following the same strategic playbook: using its high-speed HBM memory interface IP as the foundation for a broader custom silicon business, targeting Asian hyperscalers, AI labs, and fabless chip companies that lack internal silicon design teams, with its expanding IP portfolio in NoC, UCIe D2D, and LPDDR providing the same breadth of single-vendor coverage that made Broadcom indispensable to its hyperscaler customers.

Figure 31: AI Hyperscaler Custom ASIC Ecosystem

Customer	ASIC Product(s)	Code Name	IC Design Partner
Google	TPU v7 (Ironwood) TPU v8AX/v8X TPU v9p	<i>Ironwood</i> <i>Sunfish/Humufish</i> <i>Icefish</i>	Broadcom Broadcom+MediaTek Broadcom
Amazon (AWS)	Trainium 2 Trainium 3 Trainium 4	—	Marvell Alchip Alchip
Microsoft	Maia 100 Maia 200 Maia 300	— <i>Braga</i> <i>Griffin</i>	GUC GUC Marvell
Meta	MTIA 300 MTIA 400 MTIA 450–600	<i>Athena</i> <i>Iris/Iris+</i> <i>Arke/Astrid/Apollo</i>	Broadcom Broadcom —
Apple	Baltra / Sotra	—	Broadcom
xAI	X1	—	Broadcom

Source: Various, Apex Securities

Malaysia's National Semiconductor Strategy

Malaysia's semiconductor policy provides an important backdrop for SkyeChip. We think that Malaysia is emerging as a strengthening engineering base within global ASIC development workflows, with semiconductor firms actively seeking diversification beyond Taiwan and China due to geopolitical risks, rising wages, and talent shortages.

SkyeChip's average cost per engineer of approximately USD38,000 per annum is meaningfully lower than selected regional peers giving SkyeChip greater flexibility in pricing IC design services competitively while preserving strong margins. **FY26 net margin was 31.3% (RM48.5m PAT / RM155.0m revenue), among the highest in its peer group, only behind Rambus net margin of c.33%.**

Under the National Semiconductor Strategy (NSS), IC design has been designated a strategic national priority. Key developments include: (i) the USD250m decade-long Arm partnership targeting 10 local chip champions generating c.USD20bn collective annual revenue within 5–7 years; (ii) the Silicon Vision initiative transitioning from "Made in Malaysia" to "Made by Malaysia"; and (iii) incentive programmes including Pioneer Status, Malaysian Digital (MD) tax incentives, and R&D grants.

SkyeChip is one of only three initial Arm AFA recipients alongside GreatAsic and Oppstar with formal offer letters presented on 11 May 2026. On 14 April 2026, SkyeChip received conditional approval for access to both the Arm CSS and AFA platforms. The AFA definitive agreement was subsequently signed with MIDA on 23 June 2026, granting SkyeChip full access to Arm's chip design platform for product experimentation and development without upfront licensing fees, making it the second of the three recipients to formalise its access (after Oppstar on 25 May 2026). The CSS definitive agreement remains under evaluation, with management citing the scale of the undertaking and the need to ensure alignment with the government on terms before committing. AFA access typically costs millions of dollars and is rarely granted to firms outside

the largest global chip companies, and the formalisation of SkyeChip's AFA agreement confirms the scarcity value of this milestone.

Figure 32: Engineering Cost Comparison against Peers

Company	Avg Engineer Cost (USD/yr)	vs SkyeChip
ARM	USD534,172	14.1x SkyeChip
Rambus	USD205,303	5.4x SkyeChip
Alphawave (Qualcomm)	USD60,234	1.6x SkyeChip
Arteris	USD68,010	1.8x SkyeChip
Egis Technology	USD61,453	1.6x SkyeChip
Socionext	USD58,655	1.5x SkyeChip
Faraday	USD38,264	1.02x Skyechip
SkyeChip	USD37,619	1.0x (baseline)
GUC	USD36,194	0.96x SkyeChip
Brite Semicon	USD36,109	0.96x SkyeChip

Source: Companies, Apex Securities

End Market Analysis

AI/HPC and Data Centres - The Primary Growth Vector

AI and high-performance computing represent the dominant end market for SkyeChip's products. The structural shift is not merely one of scale but of architecture: the industry is migrating from monolithic GPU-centric compute towards heterogeneous chiplet-based systems, where memory interfaces and on-chip interconnects become the binding constraint on system performance. Every AI accelerator in this new paradigm requires more HBM, more sophisticated interface IP, and more die-to-die connectivity with each successive generation, creating a compounding demand curve for SkyeChip's core IP stack within what Deloitte estimates is a **c.USD500bn** AI chip market in 2026.

Two structural dynamics underpin this end market that are worth highlighting beyond the headline capex numbers. First, the AI chip product cycle has compressed dramatically to roughly 1 to 2 years versus the traditional 3 to 5-year CPU cycle (Oaklands Path), driven by the need to keep pace with explosive token demand and competitive pressure from cloud hyperscalers. This acceleration means IP providers like SkyeChip face more frequent re-licensing events per customer, not fewer, which is a fundamentally positive dynamic for recurring IP revenue. Second, the relentless pursuit of energy efficiency is forcing co-design of hardware, software, and algorithms simultaneously, which increases the complexity and specialisation of every IP block in the stack. As Jensen Huang has argued, extreme co-design is the fundamental driver of efficiency in modern computing, and every efficiency gain at the system level translates into a tighter specification for the memory interface IP that sits between the processor and HBM.

SkyeChip's revenue is overwhelmingly driven by this end market. The Group served 26 customers in FY26 (up from 14 in FY25), with the number of customers contributing 10%+ of revenue narrowing from 3 to 2, reflecting both customer base diversification and deepening of key relationships.

Memory Interface IP - Market Sizing and Generational Transition

For detailed market sizing of the HBM IP and semiconductor IP markets, refer to the Industry Analysis section. For detailed market sizing of the HBM IP and semiconductor IP markets, refer to the Industry Analysis section. In summary, the HBM IP market (USD201m in 2024, growing at

12.43% CAGR to USD513m by 2032) represents SkyeChip's core addressable segment, while the broader semiconductor design IP market reached USD8.5bn in 2024 (+20.2% YoY per IPnest), with interface IP the fastest-growing category.

What is worth adding here is the pricing dimension, which is not covered elsewhere in the report. Based on publicly available industry data compiled by Oaklands Path, current HBM3/HBM3E/HBM4 interface IP is priced at approximately **c.USD3.5m to USD5.0m** per licence, with US-headquartered providers commanding a meaningful premium. NoC and LPDDR5/5x IP starts **from c.USD0.5m to USD2.0m**. SkyeChip's blended average contract size of approximately RM7.2m (USD1.6m) across its 18-contract orderbook, which includes smaller NoC and LPDDR engagements alongside larger HBM IP deals, reflects the Group's early-stage pricing position relative to US incumbents, but with meaningful upside as silicon-proven credentials and customer references accumulate.

The pricing trajectory is structurally upward. As IP design moves to more advanced nodes, the ASP rises materially: moving from 16nm to 3nm increased chip design costs by roughly 5.6x (IBS), with software verification accounting for a disproportionate share of the escalation. (Source: Oaklands Path, Cadence) This means that each node migration not only creates a re-licensing trigger but also supports a higher licensing fee for the next-generation IP, as the value delivered to the customer in avoiding a USD50m to USD100m tapeout failure at 3nm, based on industry cost data showing 5nm tapeout alone at USD47.25m and 3nm exceeding USD100m, scales directly with the design cost itself (AllPCB)

Custom ASIC for AI and IoT

For detailed ASIC market sizing, refer to the Industry Analysis section. The key end market observation here is the customer segmentation within SkyeChip's ASIC business, which is distinct from the hyperscaler-focused IP licensing discussion that dominates the thesis narrative.

SkyeChip's ASIC business targets a structurally distinct customer segment from the hyperscaler giants that dominate the AI capex headlines. While Google, Amazon, and Microsoft command the largest individual ASIC programmes, the more compelling opportunity for a company of SkyeChip's scale lies one layer below: the rapidly expanding universe of AI startups, enterprise edge computing players, and companies across automotive, industrial, and IoT sectors that require high-performance, customised chips but lack the internal silicon design capability to build them. These companies cannot assemble a 300-person chip design team overnight, nor can they afford to fail a USD50m to USD100m tapeout and so they need a trusted external partner who brings both proven IP and full-chip design expertise under one roof. This is precisely the gap SkyeChip fills. The economics of serving this segment differ materially from the hyperscaler relationship: contract sizes are smaller, applications are more diverse, and the customer's dependency on SkyeChip as a full-service design partner is significantly deeper than a pure IP licensing transaction. That dependency is a competitive moat in its own right, it creates switching costs that extend well beyond the initial ASIC engagement.

The strategic logic of the ASIC business is best understood as a customer acquisition channel. Customers who commission a custom ASIC from SkyeChip typically become IP licensing customers for subsequent chip generations, as they integrate SkyeChip's proven IP blocks into future designs. In this way, ASIC functions as an on-ramp to the higher-margin, more scalable IP licensing core, with the upfront engineering intensity of ASIC work amortised across a longer customer lifetime value. SkyeChip's ASIC segment contributed 22.3% (RM34.6m) of FY26 revenue, up from 9.4% in FPE Oct 2025, with the RISC-V SoC contract representing a strategic expansion into full system-on-chip design.

One competitive dynamic that is underappreciated is that SkyeChip does not pursue pure design services without customers also incorporating its proprietary IP as part of the engagement. This is a deliberate strategic constraint that keeps ASIC margins higher and ensures every ASIC engagement embeds SkyeChip's IP into the customer's chip architecture, creating deep

switching costs and recurring licensing opportunities as customers return for subsequent chip generations with SkyeChip's IP already designed in.

Geographic Market - China, Taiwan, USA, Korea, and ASEAN

Geographic revenue details are covered in depth in the dedicated geographic market sections (The Chinese AI Chip Ecosystem, The US Market, Vietnam, and South Korea). In summary, the FY26 geographic mix reflects a business that is both deeply entrenched in its core China and Taiwan markets and simultaneously executing a rapid, credible diversification, with China revenue growing +43.8% YoY in absolute terms to RM97.0m (from RM67.5m in FY25) even as its revenue concentration improved materially from 73.3% in FPE Oct 2025 to 62.6% in FY26, demonstrating that diversification is being achieved through new market expansion (US surging to 23.1%, South Korea entering at 1.0%) rather than China contraction.

The most important observation for end market analysis purposes is the revenue quality signal embedded in the geographic data. The US and South Korea emerging as new markets in FY26 is not merely a diversification story, it is a product quality certification. US AI chip startups are sophisticated, well-funded buyers with access to all global IP providers including Synopsys, Cadence, and Rambus at full scale. These companies operate in the world's deepest semiconductor IP marketplace and face no geopolitical pressure to source from a Malaysian vendor and in fact, if anything, buying from a non-US provider introduces marginal procurement complexity. The fact that they are nonetheless choosing SkyeChip's interface IP is the strongest possible independent validation of its technical credibility.

South Korea reinforces the same signal through a different lens. Korean AI chip designers at Rebellions and FuriosaAI are building chips that will compete directly against NVIDIA in the global inference market. Their reputations, their investor capital, and in Rebellions' case its pending KOSPI IPO valuation, depend on getting the silicon right on the first attempt. These are not buyers who cut corners on IP quality. The emergence of Korea revenue in Q4 FY26, coinciding with SkyeChip's Samsung Foundry CONNECT listing in February 2026, suggests that the listing generated qualified Korean customer engagement almost immediately and that SkyeChip's IP passed the technical bar set by some of the most demanding chip designers in Asia.

Together, the US and Korea revenue signals matter more than their combined RM37.3m in FY26 revenue suggests. They establish that SkyeChip can compete on merit, not geopolitical convenience, in markets where the customer has every alternative available and the cost of a wrong choice is measured in tens to hundreds of millions of dollars. That is a different and more durable competitive position than one built purely on China's structural preference for non-US IP suppliers, and it is the foundation on which a premium multiple can ultimately be justified.

Competitive Landscape

Global Peers

The peer set spans four distinct archetypes, each illuminating a different dimension of SkyeChip's investment case. Arm Holdings and Rambus anchor the pure-play IP licensing comparison, validating the business model and providing valuation benchmarks for a company that designs once and licenses many. Synopsys and Cadence represent the EDA-integrated incumbents, scale players against whom SkyeChip competes selectively rather than frontally, benefiting from the geopolitical wedge that US-headquartered vendors cannot easily bridge. GUC, Faraday, and Socionext anchor the ASIC design services comparison, providing context for SkyeChip's custom ASIC segment where foundry adjacency and engineering depth drive differentiation. M31 Technology is the single most instructive comparable: a Taiwanese pure-play silicon IP house with a comparable growth profile and interface IP focus. The simple average FY27 forward P/E across the peer set is **66.1x** and FY28 forward P/E is **44.2x**, against which SkyeChip's 57.2x FY27 and 41.9x FY28 at the current price of RM2.97 represents a **14% and 5%** discount respectively.

The discount remains unjustified on fundamentals. SkyeChip enters this peer comparison with EPS growth of **36.6%** (FY27-FY28F), comparable to Arm (38.0%) and above Rambus (23.8%), Synopsys (16.5%), and Cadence (17.8%), with a net margin of 31.3% that exceeds almost every peer except Rambus, silicon-proven credentials at 4nm that most regional peers cannot match, and a US market entry that independently validates its technical quality in the world's most discerning IP marketplace. The discount reflects factors that are either already improving or structurally temporary: geographic concentration in China (declining from 90.6% to 62.6%), an early-stage listed track record (the stock has been listed for barely one month), and limited investor familiarity with a Malaysian front-end IC design company (a function of scarcity, not of quality). We see scope for progressive re-rating toward our target of **RM4.67 (76.6x mid-FY28F Core EPS)** as execution continues to de-risk these factors.

Arm Holdings is the semiconductor IP benchmark and the most watched comparable for pure-play IP licensing businesses. Arm licenses processor (CPU/GPU) IP, a fundamentally different IP category from SkyeChip, but operates the same pure licensing model with similar economics: design once, license many, collect near-pure margin on incremental licences. At 162.0x FY27 P/E and 117.4x FY28, Arm commands the highest multiple in the peer set, reflecting its monopolistic position in mobile compute (c.99%+ smartphone share), accelerating data centre and AI penetration through its Neoverse platform, and the structural shift from fixed upfront licences to per-chip royalties. Arm is relevant to SkyeChip's story on two levels: as a business model validation that IP licensing can sustain premium multiples at scale, and as the provider of the AFA and CSS frameworks that SkyeChip has signed the AFA definitive agreement (23 June 2026) and received conditional CSS approval (14 April 2026) to access, creating a potential pathway to Arm-based silicon products.

Rambus is the closest business model comparable and the most instructive direct peer for SkyeChip's valuation. Rambus designs and licenses memory interface IP (DDR, LPDDR, HBM controller, and PHY designs) alongside security IP and DDR5 Memory Interface Chips (hardware). Rambus reported FY2025 total revenue of USD707.6m (+27.1% YoY), with record product revenue of USD347.8m (+41% YoY), driven by DDR5 memory interface chip demand from AI server buildout. At 43.4x FY27 P/E and 35.1x FY28, with EPS growth of 23.8%, Rambus provides the most directly relevant valuation benchmark for SkyeChip's memory interface IP business. SkyeChip at 57.2x FY27 P/E commands a premium to Rambus's 43.4x, which we view as justified by SkyeChip's materially faster growth rate (36.6% EPS growth vs 23.8%), its ASEAN scarcity value, and its earlier-stage positioning on a steeper part of the growth curve where the IP licensing flywheel is still accelerating. The three key differences are: (i) scale, with Rambus at approximately 20x SkyeChip's revenue and a mature customer base spanning US, European, and Asian hyperscalers; (ii) geographic mix, with Rambus serving predominantly US and European customers while SkyeChip remains China-concentrated at **62.6%** though meaningfully improving; and (iii) revenue model, with Rambus earning a significant proportion from patent royalties and hardware product sales while SkyeChip focuses on upfront project-based IP licensing.

Synopsys and Cadence are the EDA/IP giants, each generating over USD5bn in annual revenue. Synopsys (FY2025 revenue USD7.054bn, +15% YoY) offers DesignWare HBM3/HBM3E/HBM4 PHY and Controller IP alongside the broadest interface IP portfolio in the industry, trading at 31.5x FY27 P/E with 16.5% EPS growth. Cadence (FY2025 revenue USD5.297bn, +14% YoY) offers DDR5/HBM3/HBM4E PHY and Controller IP, trading at 47.3x FY27 P/E with 17.8% EPS growth. Both are US-headquartered, which creates a structural headwind with Chinese customers who increasingly prefer geopolitically neutral IP suppliers, directly benefiting SkyeChip. However, their scale, breadth of IP portfolio, and the deeply embedded nature of their EDA-IP integration represent formidable barriers that SkyeChip cannot overcome at current scale. SkyeChip's competitive positioning against these incumbents is not head-on displacement but selective capture of customers who either cannot or prefer not to source from US vendors, a structurally durable niche growing rapidly as Chinese AI chip design activity accelerates.

GUC (Global Unichip) is a publicly listed Taiwanese ASIC design services company in which TSMC owns c.35% of shares. At 104.1x FY27 P/E with exceptional EPS growth of 109.8%, GUC commands the second-highest multiple in the peer set after Arm, underpinned by its privileged TSMC ecosystem adjacency that gives it access to the most advanced process nodes, guaranteed wafer capacity, and an embedded referral channel. GUC is most relevant as a comparison for SkyeChip's ASIC segment, though GUC's revenue (c.USD1bn+) dwarfs SkyeChip's and its business model is pure ASIC design services rather than IP licensing. The GUC valuation illustrates a broader principle: deep foundry ecosystem integration commands a significant premium, and SkyeChip's Samsung Foundry CONNECT listing and Intel Foundry Accelerator IP Alliance membership are early but deliberate steps toward building analogous foundry ecosystem relationships without the exclusivity constraint that limits GUC to TSMC alone.

Faraday Technology provides full-service ASIC design and silicon IP licensing, trading at 55.5x FY27 P/E with 57.8% EPS growth driven by a surge in advanced packaging mass production revenue. Its IP portfolio does not include HBM-specific memory interface capability, which is the fastest-growing segment of the semiconductor IP market. The comparison is instructive: Faraday, without HBM credentials, commands 55.8x FY27 P/E, broadly in line with SkyeChip's 57.2x, despite lower structural growth quality. SkyeChip's positioning alongside Faraday on FY27 multiples underscores the re-rating potential: as the market recognises SkyeChip's superior IP portfolio and growth profile, a premium to Faraday should widen over time.

M31 Technology is the single most directly comparable listed peer by business model: a Taiwanese pure-play silicon IP company specialising in high-speed interface IP including SerDes, DDR, USB, and PCIe alongside foundation IP. At 66.3x FY27 P/E with 65.0% EPS growth, M31 trades at a modest premium to SkyeChip's 57.2x, a gap that we view as reflecting M31's longer listed track record and Taiwanese domicile rather than any fundamental difference in business quality. SkyeChip's IP portfolio is in fact broader and more technically advanced than M31's, with HBM3/HBM3E credentials and NoC and D2D coverage that M31 does not offer. On FY28 P/E, SkyeChip trades at 41.9x versus M31's 40.2x, a marginal premium that reflects SkyeChip's faster absolute growth and ASEAN scarcity.

Socionext is a Japanese fabless semiconductor company designing custom SoCs for automotive, data centre, and networking applications. At 33.3x FY27 P/E with 49.0% EPS growth on approximately USD1.5bn revenue, Socionext provides the lower bound of our peer range, reflecting its mature revenue profile, Japanese-market concentration, and a business model weighted toward production silicon rather than IP licensing. The gap between SkyeChip at 57.2x and Socionext at 33.3x is justified by SkyeChip's IP-first model, substantially higher margin structure, and the ASEAN scarcity premium.

Regional Peers - The Malaysian IC Design Landscape

Oppstar (OPPSTAR MK) is the only other meaningful Malaysian-listed IC design company but occupies a fundamentally different investment category. Oppstar reported PAT losses in its most recent financial year (PAT -RM10.7m vs +RM20.8m in the prior year), with a market capitalisation of c.RM503.5m as at 18 May 2026. The contrast with SkyeChip is stark: SkyeChip generated FY26 PAT of RM48.5m (+35% YoY), commands a RM1,580m market capitalisation, possesses silicon-proven HBM3E, NoC, and D2D interface IP that Oppstar does not offer, and is actively expanding into new geographies (US: 23.1% of FY26 revenue; South Korea: new market in Q4 FY26). Both companies received AFA offer letters on 11 May 2026 under the Arm-Malaysia programme, but they represent categorically different investment propositions.

The broader Malaysian semiconductor sector which is dominated by OSAT companies (Inari Amertron, Unisem, MPI), equipment manufacturers (Greatech, ViTrox, Pentamaster), and materials companies which operates predominantly in the back-end of the value chain, processing chips designed elsewhere. SkyeChip's listing represents a genuine structural addition to the Bursa Malaysia semiconductor universe: the first profitable, pure-play front-end IC design and IP licensing company at meaningful scale. This scarcity commands a premium that we

believe the market has not yet fully priced in a point developed in Investment Thesis #5 (ASEAN Scarcity Premium).

GreatAsic Technology is a privately held Malaysian IC design company and the only one of the three Arm token recipients to receive both AFA and CSS access suggesting more advanced compute SoC capabilities than either SkyeChip or Oppstar at present. As a private company it provides no public market comparison. Should GreatAsic pursue a listing in due course, it would represent a more direct competitive comparison for SkyeChip's higher-end ambitions, particularly if the CSS access translates into a commercially deployed server-grade CPU or AI platform product.

SkyeChip's Competitive Positioning

SkyeChip occupies a distinctive and defensible niche: a high-growth, pure-play memory interface and interconnect IP company with disproportionate exposure to the Chinese AI chip ecosystem, emerging US market penetration, and an expanding geographic base that is diversifying at pace.

Competitive advantages:

(i) **Silicon-proven HBM3E IP at 4nm.** SkyeChip achieved first-time silicon success at 8,800 Mbps on Samsung SF4X (LN04LPP), making it one of a very small number of companies globally with commercially deployed HBM3E interface IP at an advanced process node. In a market where IP quality is ultimately verified by the willingness of sophisticated customers to risk USD50-100m tapeouts on it, silicon-proven status is the defining and hardest-to-replicate moat. Customers licensing critical interface IP for chips of that cost do not use unproven designs, and replicating SkyeChip's 4nm HBM3E track record requires years of accumulated engineering expertise, advanced foundry PDK access, and multiple tapeout cycles that cannot be shortcut.

(ii) **Broadest IP portfolio in its size class.** SkyeChip offers memory interface IP (HBM3/HBM3E with HBM4 in progress, DDR5, LPDDR5 with LPDDR6 in progress), NoC IP with the proprietary RAPTuner EDA tool bundled, UCIe-compliant D2D interface IP, and full custom ASIC design services, all from a single vendor. SkyeChip has the broadest memory IP coverage among listed peers of comparable scale, spanning HBM3, HBM3E, DDR5, LPDDR5, NoC, D2D, and UCIe. Most peers of comparable scale specialise in two to three of these categories. Single-vendor coverage reduces integration risk for customers, increases switching costs once IP is embedded in a chip design, and creates natural cross-selling opportunities as customers expand their IP requirements across generations.

(iii) **Geopolitical positioning as a structural moat.** As a Malaysian-incorporated company with no US-origin technology restrictions, SkyeChip sits in the gap created by US export controls on advanced AI chips and EDA tools. Chinese AI chip designers who cannot or prefer not to source from US-domiciled IP vendors have very few alternative providers of validated HBM interface IP at advanced process nodes. This is a structural competitive advantage that does not require active management to maintain and will persist as long as US-China technology tensions remain elevated, which the current geopolitical trajectory suggests is a multi-year condition rather than a temporary one. Critically, SkyeChip's geopolitical neutrality works in both directions: it can serve Chinese customers without restriction and US customers without the geopolitical sensitivity that attaches to a Chinese IP vendor.

(iv) **Multi-foundry access and portability.** SkyeChip has secured PDK access from multiple leading foundries enabling IC design down to 3nm, including TSMC (where its first-generation HBM IP was taped out on TSMC 12nm) and Samsung Foundry (where HBM3E was silicon-proven at SF4X 4nm and UCIe-AP 32G PHY IP is now listed on Samsung CONNECT). Access to Intel Foundry's process technologies was formalised in January 2025 through the Intel Foundry Accelerator IP Alliance. This foundry portability is a meaningful commercial differentiator that gives customers a credible alternative manufacturing path, a "Plan B" that has real value when leading-edge capacity is constrained.

(v) **Samsung Foundry CONNECT as a zero-cost commercial channel.** SkyeChip's UClE Advanced Package 32G PHY IP was officially listed on Samsung Foundry CONNECT on 16 February 2026, implemented on Samsung SF4X (4nm) and designed for 32GT/s UClE Advanced Package applications. This listing enables every Samsung Foundry customer globally to discover, evaluate, and engage with SkyeChip directly through Samsung's own IP ecosystem platform, at zero incremental cost to SkyeChip and without requiring a local sales office. The timing is notable: the listing occurred in February 2026, within Q4 FY26 (January to March 2026), which is the same quarter SkyeChip first recorded South Korea revenue of c.RM1.5m (1.0% of Group revenue), suggesting the channel began generating customer engagement shortly after going live.

(vi) **ASEAN scarcity value.** SkyeChip is the only profitable, pure-play front-end semiconductor IP company listed across ASEAN exchanges, with no direct listed comparable in the region. The Malaysian semiconductor sector is dominated by OSAT companies, equipment manufacturers, and materials suppliers, all operating majority in the back-end of the value chain. SkyeChip's front-end positioning and IP ownership model are genuinely unusual within the ASEAN listed universe, and scarcity commands a structural premium in capital markets, as the Arm Holdings experience demonstrated when it listed on NASDAQ in September 2023 as the only large-cap pure-play IP licensor available publicly. This point is developed in Investment Thesis #5.

(vii) **Arm AFA access secured, CSS approval conditional.** SkyeChip signed the definitive agreement for access to the Arm Flexible Access (AFA) platform with MIDA on 23 June 2026, formalising the conditional approval received on 14 April 2026. AFA grants access to Arm CPU cores (Cortex-M and Cortex-A series), Mali GPU, TrustZone, and AMBA interconnect for IoT and edge computing applications, and is now fully executable. The Arm Compute Subsystem (CSS) platform, which grants access to Neoverse server-grade compute subsystems for high-performance CPU and AI platform development, remains at the conditional approval stage, with the Group still evaluating the terms and conditions of the definitive agreement given the scale of the undertaking and the costs involved. If the CSS definitive agreement is finalised, it opens a pathway from IP licensor to silicon product company, following the same trajectory that Arm's largest licensees used to build billion-dollar businesses, with RM82.0m of IPO proceeds ring-fenced for this purpose. We have not included any AFA or CSS-related revenue in our base case forecasts, but we view the AFA execution as a meaningful de-risking event and the pending CSS resolution as a medium-term catalyst that is currently not priced into the market.

Competitive Vulnerabilities:

(i) **Scale disadvantage relative to global incumbents.** At RM155.0m FY26 revenue (c.USD35m), SkyeChip is approximately 20x smaller than Rambus (USD707.6m FY2025), approximately 200x smaller than Synopsys (USD7.054bn FY2025), and approximately 150x smaller than Cadence (USD5.297bn FY2025). This limits R&D capacity for new IP categories, creates pricing pressure on large enterprise contracts where Synopsys and Cadence cross-subsidise IP pricing with EDA tool revenue, and restricts the depth of customer-facing technical support and account management relative to the largest players. Scale is earned over time through execution, and SkyeChip's FY23-FY26 CAGR of 39.6% is narrowing the gap rapidly, but the disadvantage is real at present.

(ii) **Geographic concentration remains the primary risk.** China and Taiwan together at 73.8% of FY26 revenue, while significantly improved from 90.6% in FPE Oct 2025, remains the single most important risk factor for the investment case. Any deterioration in Chinese AI chip design activity, whether from domestic policy shifts, a slowdown in AI capex, or escalating US sanctions specifically targeting Malaysian intermediaries in the semiconductor IP supply chain, would materially impact Group earnings. The FY26 trajectory is constructive on both dimensions simultaneously: China revenue grew +43.8% YoY in absolute terms (RM97.0m vs RM67.5m) while its share of total revenue declined from 73.3% to 62.6%, demonstrating that diversification is being achieved through new market expansion rather than China contraction.

(iii) **Upfront licensing model forfeits production volume participation.** SkyeChip's project-based, lump-sum licensing structure front-loads revenue recognition and provides relatively

stable NRE-driven cash flows but forfeits participation in customers' production volume upside. As customers ramp from prototype to mass production, and as Chinese AI chip volumes scale from development samples to commercial deployment, the absence of a per-chip royalty component means SkyeChip does not participate in that compounding. Rambus, by contrast, derives a significant proportion of revenue from recurring patent royalties and per-unit hardware product sales. The potential transition towards royalty-based arrangements as SkyeChip's customer base matures and production volumes become more predictable represents a meaningful medium-term revenue upside scenario that is not reflected in our base case forecasts.

(iv) **Customer commercialisation uncertainty.** Several of SkyeChip's customers are early-stage AI chip companies with uncertain production timelines and volume ramp profiles. Project-based revenue recognition provides some insulation since revenue is earned on engineering milestones rather than customer production success, but customer attrition among newer accounts, or a broader slowdown in Chinese AI chip investment activity, remains a tail risk. The FY26 customer base expansion from 14 to 26 customers, alongside the reduction in the number of customers contributing more than 10% of revenue from 3 to 2, suggests improving diversification within the customer base itself.

(v) **CSS definitive agreement still pending.** On 23 June 2026, SkyeChip signed the definitive agreement for access to the Arm Flexible Access (AFA) token with MIDA, formalising the conditional approval received on 14 April 2026 and granting full access to Arm's chip design platform for experimentation and development without upfront licensing fees. This de-risks one of the two key optionality pathways in our thesis. However, the definitive agreement for the Arm Compute Subsystem (CSS) token remains pending, with CEO Datuk Fong Swee Kiang citing the scale of the undertaking and the need to ensure alignment with the government on terms before committing. If the CSS agreement cannot be finalised on acceptable terms, the server-grade CPU and AI platform pathway (RM82.0m of IPO proceeds ring-fenced) would not be available and SkyeChip would pursue RISC-V-based or other architectural alternatives. We view the AFA execution as a meaningful positive catalyst, while CSS resolution remains the key outstanding variable.

vi) **EDA Tool Concentration Risk.** Synopsys, Cadence, and Ansys (now part of the Synopsys group following acquisition completion in July 2025) dominate SkyeChip's IC design toolchain, collectively accounting for approximately 60.6% of total operational costs and 7.3% of cost of sales in FPEOct 2025. Any tightening of US Bureau of Industry and Security (BIS) export controls on EDA tools could introduce operational disruption to SkyeChip's design workflow, though the Group has begun onboarding Cadence as an alternative EDA provider to partially mitigate concentration in Synopsys tools, and is developing its own proprietary RAPTuner tool for NoC IP workflows.

Competitive Positioning Summary

On balance, SkyeChip's competitive positioning is strong within its chosen niche, and we view the competitive advantages outlined above as genuinely durable rather than transitional. The key question for investors is whether the Group can sustain its exceptional revenue growth trajectory (FY23-FY26 CAGR of **c.39.6%**, with FY26 revenue of RM155.0m and PAT of RM48.5m) while simultaneously diversifying its customer and geographic base and executing its technical roadmap across HBM4, LPDDR6, 2nm node migration, RISC-V, and automotive IP. The stock has re-rated substantially since listing, from the IPO price of RM0.88 to RM2.97 (+237%) and now trades at 57.2x FY27 P/E and 41.9x FY28 P/E, a **14% and 5%** discount to the peer simple averages of 66.1x and 44.2x respectively. We believe the re-rating validates the market's recognition of the IP licensing model and ASEAN scarcity premium, but does not yet fully reflect SkyeChip's superior growth profile (**FY26-29F core earnings CAGR of c.48%**), its unpriced optionality from the signed AFA definitive agreement (23 June 2026), conditional Arm CSS approval, and Samsung Foundry CONNECT channel, or the continued geographic de-risking as China concentration declines. Successful execution on this trajectory, combined with progressive reduction in China revenue concentration and the potential formalisation of CSS access, would warrant further re-rating

beyond current levels. Our target price of **RM4.67**, based on 76.6x mid-FY28F Core EPS (a **15% premium to the 66.1x peer average**), implies **57% upside** from the current price and is achievable as SkyeChip demonstrates execution consistency over the next two to three reporting periods and the market progressively de-risks the China concentration, Pioneer Status renewal, and early-stage track record factors that currently constrain the multiple.

Figure 33: Skyechip vs Global Peers Scorecard

Dimension	SkyeChip	Rambus	Synopsys	Cadence	M31 Tech	GUC
HBM Interface IP Depth	5	4	5	4	2	3
Portfolio Breadth	4	3	5	5	3	4
Geographic Revenue Reach	2	5	5	5	3	4
Geopolitical Neutrality	5	2	1	1	2	2
Multi-Foundry Access	5	3	4	4	3	2
Revenue Growth Rate (3Y CAGR)	5	3	3	3	3	3
Average Score (out of 5.0)	4.3	3.3	3.8	3.7	2.7	3.0

Source: Companies, Apex Securities

Figure 34: Skyechip Competitive Advantages and Vulnerabilities

COMPETITIVE ADVANTAGES				
	Advantage	Why It Matters	Moat Type	Status
i	Silicon-proven HBM3E at 4nm	First-time silicon success at 8,800 Mbps (SF4X). Customers risk USD50-100m tapeouts - proven IP is non-negotiable.	Structural Moat	<i>Deployed commercially</i>
ii	Broadest portfolio in size class	HBM3/3E, DDR5, LPDDR5, NoC, UCIe D2D, ASIC — all one vendor. Broadest memory IP coverage among listed peers (Kenanga Exhibit 11).	Earned Moat	<i>HBM4/LPDDR6 in progress</i>
iii	Geopolitical neutrality	Malaysian domicile = no US export restrictions. Chinese AI designers prefer non-US vendors. Works in both directions: US and China.	Structural Moat	<i>Requires no active mgmt</i>
iv	Multi-foundry access	Qualified IP on TSMC (HBM3, 12nm+), Samsung SF4X (HBM3E, 4nm), Intel Foundry (18A/14A via alliance). GUC is TSMC-only.	Earned Moat	<i>3 foundries; rare at this scale</i>
v	Samsung Foundry CONNECT	UCIe-AP 32G PHY listed Feb 2026. Zero-cost channel to every Samsung Foundry customer globally. Korea revenue followed in same quarter.	Earned Moat	<i>Already converting</i>
vi	ASEAN scarcity premium	Only profitable pure-play front-end IP company listed in ASEAN. No direct regional comparable. Scarcity commands structural premium.	Structural Moat	<i>No comparable listed peer</i>
vii	Arm AFA + conditional CSS	Conditional approval 14 Apr 2026 for both. CSS opens Neoverse server-grade platform pathway, potential silicon product company.	Earned Moat	<i>Definitive agmt not yet signed</i>

	Vulnerability	Key Risk	Severity
i	Scale vs global incumbents	20x smaller than Rambus, 200x smaller than Synopsys. Limits R&D breadth and enterprise account depth.	HIGH Severity
ii	China geographic concentration	62.6% of FY26 revenue. US sanctions escalation targeting Malaysian IP intermediaries is primary tail risk.	HIGH Severity
iii	No royalty / upfront model only	Lump-sum NRE forfeits per-chip royalty upside as customers ramp to mass production. Rambus earns recurring royalties.	MEDIUM Severity
iv	Customer commercialisation risk	Several customers are early-stage AI chip companies with uncertain production timelines and volume ramp profiles.	MEDIUM Severity
v	AFA/CSS definitive agmts unsigned	Conditional approval only as at 18 May 2026. If CSS terms fail, server-grade CPU/AI platform pathway unavailable.	MEDIUM Severity
vi	EDA tool concentration	Synopsys + Ansys (merged) and Cadence = c.60.6% of operational costs. US BIS EDA tool controls are an emerging risk.	LOW Severity

Source: Company, Apex Securities

Financial Highlights

SkyeChip has delivered strong and accelerating financial performance, with revenue growing from RM57.2m in FY23 to RM155.0m in FY26, a three-year CAGR of **c.39.6%**, while PAT expanded from RM28.6m to RM48.5m over the same period (three-year CAGR: 19.3%). The PAT CAGR of 19.3% appears modest relative to the c.39.6% revenue CAGR but reflects a specific margin compression cycle in FY24-FY25 as the custom ASIC segment ramped and gross margin declined from 59.1% in FY23 to 42.2% in FY25 before recovering materially to 45.1% in FY26, reversing the compression trend and establishing an improved base from which PAT growth should accelerate. Most notably, Q4 FY26 alone contributed RM58.9m in revenue and RM31.5m in PAT representing 38% of full-year revenue and 65% of full-year PAT in a single quarter. We view this as a quarterly profile that indicates a business entering a steeper part of its growth curve as operating leverage materialises across a broader customer and geographic base. The operational metrics corroborate the trajectory: the customer base nearly doubled from 14 to 26 in FY26 while top-customer concentration improved (2 customers at 10%+ vs 3 in FY25), and US revenue surged from 5.7% (FPE Oct 2025) to 23.1% of Group revenue (RM35.8m) in FY26, establishing in the world's most demanding semiconductor IP market that SkyeChip can win on merit rather than geopolitical preference alone.

Figure 35: Income Statement Summary (FY23-FY26)

FYE March (RM'm)	FY23	FY24	FY25	FY26	YoY %	3yr CAGR
Revenue	57.2	77.1	119.5	155.0	+29.7%	39.6%
Gross Profit	33.8	36.0	50.4	69.9	+38.7%	27.2%
GPM (%)	59.1%	46.8%	42.2%	45.1%	+2.9pp	
Operating Profit	28.0	33.6	36.5	49.2	+34.8%	20.7%
PBT	28.4	34.6	37.0	50.0	+35.3%	20.8%
Tax (expense) / credit	0.2	(0.9)	(1.1)	(1.5)		
PAT	28.6	33.7	35.9	48.5	+35.0%	19.2%
PAT Margin (%)	50.1%	43.7%	30.1%	31.3%	+1.2pp	
EPS (sen)	1.6	1.9	2.0	2.7	+35.0%	19.2%
Eff. Tax Rate (%)	-0.9%	2.5%	2.9%	3.0%		

Source: Company, Apex Securities

Revenue. FY26 revenue of RM155.0m represented a **29.7%** increase from RM119.5m in FY25, driven by: (i) a 39.3% surge in silicon IP revenue to RM119.4m (77.0% of total), reflecting a larger number of projects and customers secured for standard memory interface IPs and new D2D interface IP; (ii) an 8.5% increase in custom ASIC revenue to RM34.6m (22.3% of total), proving more resilient than the FPE Oct 2025 data initially suggested; and (iii) the emergence of the US as 23.1% of Group revenue (RM35.8m), up from 5.7% in FPE Oct 2025. The customer base nearly doubled to 26 (from 14 in FY25), with new markets in the US and South Korea contributing 24.1% of FY26 revenue. The revenue trajectory was heavily back-end loaded: Q1-Q3 FY26 generated RM96.1m (62% of full-year revenue) while Q4 FY26 alone contributed **RM58.9m** (38% of full-year), underscoring the lumpiness inherent in a project-based IP licensing business where milestone deliveries can concentrate in specific quarters. Q4's exceptional performance was driven by US revenue of RM28.9m (49% of Q4 revenue), a single quarter of US revenue that nearly matched SkyeChip's entire FY25 quarterly average of RM29.9m across all geographies.

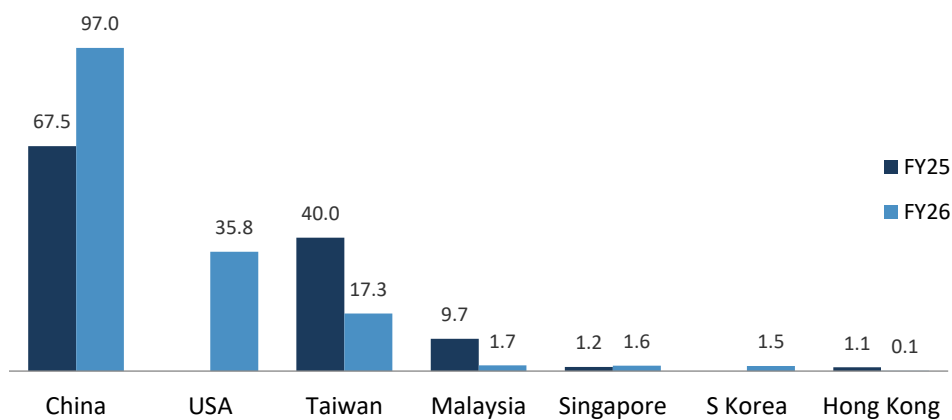
Gross margin. FY26 GPM improved to 45.1% from 42.2% in FY25, reversing two years of compression from the 59.1% peak in FY23. Notably, this improvement occurred despite a higher ASIC revenue share (22.3% vs 9.4% in FPE Oct 2025), suggesting IP licensing margins are expanding as the portfolio scales and IP reuse economics improve. Based on our segment-level estimates, silicon IP GPM was approximately 46.6% and custom ASIC GPM was approximately 41.8% in FPE Oct 2025, with the blended FY26 improvement suggesting both segments contributed positively. Q4 FY26 gross margin of 64.0% (RM37.7m GP on RM58.9m revenue) is the

standout quarterly data point, representing more than 18 percentage points above the full-year average of 45.1% and a step-up from the Q1-Q3 FY26 blended GPM of approximately 33.5%. This likely reflects a favourable concentration of high-margin standard IP licensing deliveries in the quarter, with US customer IP deliveries (RM28.9m of Q4 revenue) as the primary driver. If Q4 FY26 is indicative of the margin profile achievable as the IP portfolio and US customer mix deepens, the GPM trajectory for FY27 has meaningful upside relative to the FY26 full-year average.

Operating expenses. Administrative expenses rose to RM22.3m in FY26 (14.4% of revenue) from RM15.5m in FY25 (13.0%), reflecting higher directors' remuneration, increased amortisation charges from the tripling of the intangible asset base to RM22.2m as IP development costs were capitalised, a sharp increase in realised FX losses to RM3.2m (vs RM1.2m in FY25), and increased staff costs as the engineering team expanded. Employee benefits expenses reached RM73.1m (up from RM60.1m in FY25, +21.6%), but as a proportion of revenue declined from 50.3% to 47.2%, a positive signal that revenue growth is outpacing headcount cost growth and operating leverage is building.

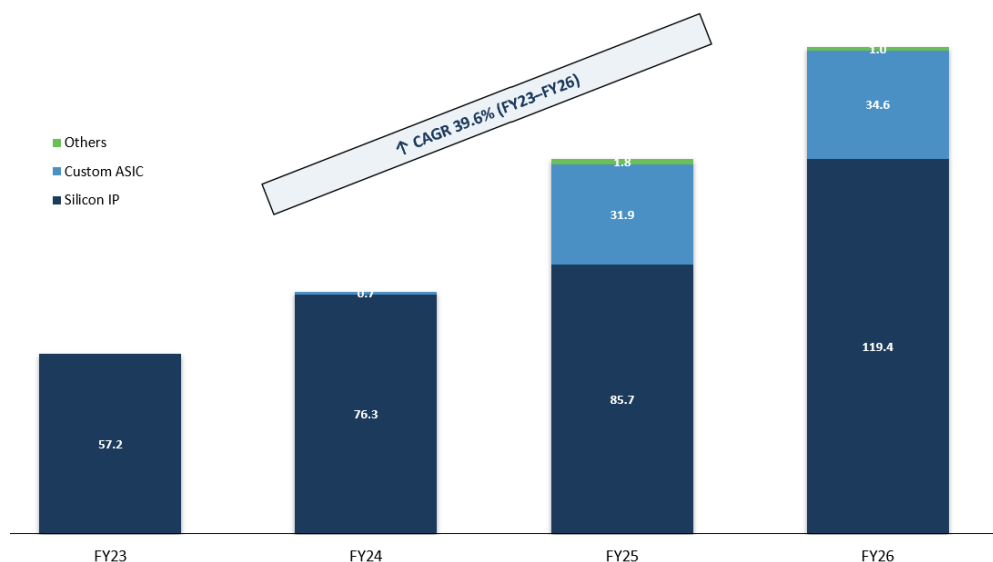
PAT. FY26 PAT of RM48.5m grew 35.0% from RM35.9m in FY25, with PAT margin stabilising at 31.3% (vs 30.1% in FY25). The effective tax rate of 3.0% was better than the prospectus guidance of approximately 5.0%, benefiting from the Section 127(3A) Pioneer Status exemption covering the majority of FY26 (expired 9 September 2025) and Vietnam operations enjoying a five-year corporate income tax exemption commencing May 2025. The quarterly PAT profile is exceptional. Q1 to Q3 FY26 combined generated only RM17.0m (35% of full-year PAT), while Q4 FY26 alone delivered RM31.5m (65% of full-year PAT). The Q4 PAT margin of 53.5% was over 22 percentage points above the full-year average. Annualised, Q4 FY26 implies approximately RM126m in annual PAT, which we do not use as our base case given the lumpiness of IP delivery timing, but which nonetheless anchors the earnings power of the business at scale when operating leverage is fully engaged.

Figure 36: Geographic Revenue FY25 vs FY26



Source: Company, Apex Securities

Figure 37: Revenue Breakdown by Segment (FY23-FY26)



Source: Company, Apex Securities

Earnings Outlook (FY27F-FY29F)

We forecast SKYECHIP's core earnings to grow at a 47.5% CAGR over FY26A-FY29F, with core net profit accelerating from RM49.7m (FY26A) to RM93.2m (FY27F, +87.5%), RM127.3m (FY28F, +36.6%), and RM159.6m (FY29F, +25.4%), driven by: (i) continued ramp of HBM3E and next-generation HBM4 IP licensing as Chinese, American, and Korean AI chip customers enter new design cycles; (ii) custom ASIC project completions and new contract wins including AI inference and RISC-V SoC engagements; (iii) geographic diversification with the US sustaining its trajectory as the fastest-growing market and South Korea scaling from its Q4 FY26 entry point; (iv) operating leverage as gross margin expands from 45.1% (FY26A) to 48.6% (FY27F) and 50.9% (FY29F) on the IP licensing flywheel; and (v) a step-change in finance income from RM1.1m to RM6.6m as the RM434m post-IPO cash balance earns interest.

Key Drivers. Revenue is forecast at RM212.9m (FY27F, +37.4%), RM276.0m (FY28F, +29.6%), and RM344.9m (FY29F, +24.9%), representing a five-year CAGR of 26.6% to RM504.5m by FY31F. The deceleration from 37.4% to 19.9% reflects the mathematical reality of a growing base and our assumption that SkyeChip's extraordinary share-gain phase gradually converges toward a more sustainable 1.5-2.5x market growth multiple. Gross margin expansion from 45.1% to 54.7% over the forecast period is driven by the IP reuse economics: revenue per engineer rises from RM425k (FY26A) toward RM690k+ by FY31F as each silicon-proven IP block is licensed to progressively more customers with near-zero marginal cost, though the key risk is EDA tool cost inflation (M31 Technology cited over 50% YoY growth in advanced-node EDA expenses as a peer-confirmed margin headwind). Administrative expenses normalise from 14.4% of revenue (FY26A) to 8.3% (FY27F) as one-off FX losses and IPO preparation costs drop out, then compress further to 6.4% by FY31F as semi-fixed costs are spread across a larger revenue base, representing substantial operating leverage worth approximately RM5m per percentage point of compression on a RM500m revenue base.

Q4 Implications. Q4 FY26 delivered RM58.9m in revenue (38% of full-year), RM31.5m in PAT (65% of full-year), and a 64.0% gross margin, all record quarterly results by a substantial margin, with US revenue of RM28.9m alone (49% of Q4 revenue) representing a single-quarter run-rate that nearly matched SkyeChip's entire FY25 quarterly average across all geographies. Annualised, Q4 implies approximately RM235.6m in revenue and RM126.0m in PAT, well above our FY27F forecast of RM212.9m and RM90.2m respectively. We do not annualise Q4 as our base case given the inherent lumpiness of project-based IP licensing, and the 64.0% GPM is unlikely to be sustained as the segment mix normalises to include lower-margin ASIC deliveries. However,

the data point validates three important signals: (i) the addressable market supports RM55-60m quarterly revenue, underpinning the RM200m+ FY27F target; (ii) gross margins of 60%+ are achievable in IP-heavy quarters, suggesting our 48.6% FY27F GPM may prove conservative; and (iii) the US market is capable of generating RM25-30m per quarter (RM100-120m annualised), confirming SkyeChip can compete on merit in the world's most demanding semiconductor IP marketplace.

Revenue Bridge. We bridge FY26A revenue of RM155.0m to FY27F of RM212.9m (+RM57.9m or +37.4%) across three pillars: (i) silicon IP growth of approximately RM22.6m (39% of the bridge), with silicon IP revenue rising from RM119.4m to approximately RM142.0m (+18.9%) driven by new HBM3E/HBM4 licensing deals, NoC IP expansion against Arteris in a **11-16%** CAGR market, and D2D/UCle scaling via Samsung Foundry CONNECT referrals, with the unbilled silicon IP orderbook of RM52.3m providing approximately 37% baseline coverage; (ii) custom ASIC growth of approximately RM30.4m (53% of the bridge), with ASIC revenue surging from RM34.6m to approximately RM65.0m (+87.9%) as AI inference and RISC-V SoC contracts enter peak revenue recognition, supported by TrendForce's projection that custom ASIC shipments from cloud providers will grow 44.6% in 2026; and (iii) others and geographic mix contributing approximately RM4.9m (8% of the bridge) as Vietnam-sourced revenue begins scaling toward management's 12-17% medium-term target. The unbilled orderbook of RM130.3m as at 31 March 2026, comprising RM52.3m from silicon IP and RM78.0m from custom ASIC and other segments, with approximately RM94.6m (73%) expected to be recognised in FY27, provides 44.4% baseline coverage of our FY27F revenue forecast, leaving approximately RM118.3m to be secured from new contracts during the year.

Orderbook coverage provides 44.4% baseline visibility: the RM130.3m unbilled orderbook with approximately RM94.6m expected in FY27 leaves approximately RM118.3m to be secured from new contracts, equivalent to 16-17 new contracts at the current average contract value of RM7.2m. Given the customer base expansion from 14 to 26 in FY26 and established pipeline channels (Samsung CONNECT, Intel Foundry Alliance, US/Korea market channels), we view this as achievable, though it represents execution risk investors should monitor through quarterly orderbook disclosures. We forecast customers expanding from 26 (FY26) to 32-35 (FY27F) and 40-45 (FY28F), with the US contributing 3-5 new customers per year and the K-Nvidia ecosystem and Big Fund III deployment driving Korean and Chinese customer additions respectively.

Earnings Sensitivity. Revenue variance: every 5% deviation from our RM212.9m forecast translates to approximately RM5.0m at PAT; a 10% miss to RM191.6m would reduce PAT to approximately RM80.2m (EPS 4.47 sen), while a 10% beat to RM234.2m would lift PAT to approximately RM100.2m (EPS 5.58 sen). Gross margin variance: every 1pp deviation from our 48.6% GPM impacts gross profit by approximately RM2.1m; if GPM reverts to FY26's 45.1%, PAT would decline by approximately RM7.2m, while if Q4 FY26's 64.0% signals a structural shift and full-year GPM reaches 52%, PAT would increase by approximately RM7.0m. Tax rate variance: the ETR swing from our 4.0% base case to the worst-case 22% would reduce PAT by approximately 19% to RM73.3m. FX impact: a 5% Ringgit strengthening against the USD would create approximately RM5-8m in combined PAT headwinds from FX losses and revenue translation, and with approximately 97% of revenue in foreign currencies and no hedging programme in place, the FX sensitivity is material. Finance income variance: the combined swing range on our RM6.6m assumption is approximately RM4.0m to RM9.0m depending on BNM rate movements (plus/minus 50bps) and IPO proceeds deployment timing.

Tax Exemption Deep Dive

SKYECHIP has historically enjoyed a near-zero effective tax rate under a Section 127(3A) Pioneer Status exemption granted by the Malaysian government for IC design and IP activities. This exemption expired on 9 September 2025 and the renewal application, submitted to MIDA on 9 June 2025, remains under review. **The standard Malaysian corporate tax rate is 24%. This is a binary risk that materially impacts earnings.**

FY26 actual. The effective tax rate for FY26 was 3.0% (RM1.5m tax on RM50.0m PBT), better than the prospectus guidance of approximately 5.0% or less. This reflected: (i) the exemption covering the majority of FY26 (first 5 months of the fiscal year); and (ii) Vietnam operations benefiting from a 5-year corporate income tax exemption commencing May 2025. In the event the MIDA renewal is denied, the Group has indicated it will apply for Malaysian Digital (MD) tax incentives from MDEC as a fallback.

Base-case rationale. We assume full renewal given: (i) Malaysia's active policy push for semiconductor development under the National Semiconductor Strategy (NIMP 2030), with IC design explicitly designated as a strategic national priority; (ii) SkyeChip's status as one of only three initial Arm AFA token recipients and conditional approval for CSS platforms (14 April 2026) under the Malaysia Silicon Vision partnership; (iii) the government's track record of supporting high-tech Pioneer Status companies, reinforced by the Economy Minister publicly championing SkyeChip at the 11 May 2026 token ceremony; and (iv) the precedent set by SkyeChip's receipt of Malaysia Digital Status from MDEC, which provides a fallback pathway that alone would limit the effective rate to approximately 12%. The Vietnam 5-year tax exemption (commencing May 2025) provides a structural shield on an estimated 12-15% of Group profit regardless of the Malaysian outcome. Our base case effective tax rate of 4.0% for FY27F (RM3.8m tax on RM94.0m PBT) is modestly above the FY26 actual of 3.0%, reflecting the taxability of post-IPO finance income at the full 24% statutory rate even under Pioneer Status. We estimate that a normalised 24% tax rate scenario, representing a true worst case, would reduce FY27F PAT by approximately 19% from RM90.2m to RM73.3m and EPS from 5.02 sen to 4.08 sen

Balance Sheet

SkyeChip maintains an exceptionally strong balance sheet with minimal gearing and substantial cash reserves, reflecting the capital-light economics of an IP licensing business where R&D spend is the primary investment and physical asset intensity is low.

Cash and liquidity. As at 31 March 2026 (pre-IPO), the Group held RM82.6m in cash and bank balances (up from RM42.5m in FY25, +94.4% YoY), generating a pre-IPO net cash position of RM77.4m after deducting RM5.3m in total borrowings (all lease liabilities, zero financial debt). Post-IPO, with RM352m in gross proceeds added to the existing RM82.6m cash position, the Group will hold approximately RM434m in gross cash with effectively zero financial debt, giving it one of the strongest balance sheets of any Bursa-listed technology company at comparable market capitalisation.

Gearing and leverage. Total borrowings of RM5.3m represent exclusively lease liabilities with zero bank borrowings or debt financing. The debt-to-equity ratio of 2.7% (RM5.2m / RM195.7m) is negligible by any benchmark. Pre-IPO net cash to equity of 39.5% (RM77.4m / RM195.7m) indicates the Group is a significant net cash generator. Post-IPO this strengthens further to approximately 215% of pre-IPO equity, providing exceptional financial flexibility for the R&D investment programme funded by IPO proceeds.

Profitability ratios. Return on equity (ROE) of 30.1% (FY26 PAT RM48.5m / average equity RM161.0m) is exceptional for a Malaysian-listed technology company and reflects the near-pure-margin economics of standard IP licensing once the portfolio has been developed and silicon-proven. Return on assets (ROA) of 26.7% (FY26 PAT / average assets RM181.7m) confirms that assets are being deployed productively. Asset turnover of **0.85x** is appropriate for an IP-intensive business where intangible assets (R&D capitalisation) represent a significant and growing proportion of the asset base.

Working capital and receivables. Trade and other receivables grew 46.6% to RM51.6m, outpacing revenue growth of 29.7%, suggesting limited deterioration in collection quality. Receivables days of approximately 121 days (RM51.6m / RM155.0m x 365) reflects the project-based nature of IP licensing contracts, where payment schedules are tied to longer milestone deliveries rather than standard 30-60 day invoice terms. Contract assets grew substantially to RM7.1m (from RM0.5m in FY25), consistent with an acceleration of project activity in the second

half of FY26. The concentration of receivables is improving: 2 customers contributed RM47.4m or 10%+ of revenue in FY26 (down from 3 customers contributing RM72.2m in FY25), indicating that the receivables book is less concentrated even as its absolute size grows.

Intangible assets, R&D capitalisation and PPE. Intangible assets increased 3.5x to RM22.2m (from RM6.4m in FY25), with gross additions of approximately RM17.6m during FY26 before approximately RM1.8m in amortisation charges. This capitalisation reflects IP development costs for next-generation products including HBM4, LPDDR6, and automotive-grade NoC IP expenditure that should translate into future revenue streams as these IP blocks are silicon-proven and licensed commercially. The growth in capitalised intangibles is a leading indicator of the Group's forward IP pipeline and is consistent with the RM211.5m of IPO proceeds earmarked for direct R&D expenditure over 36 months. Plant and equipment also grew 23.6% to RM48.2m, reflecting investment in EDA computing infrastructure and leasehold improvements as the Group scales its engineering capacity.

Equity and NAV. Total equity grew 55.0% to RM195.7m (from RM126.3m in FY25), driven largely by retained earnings from FY26 PAT of RM48.5m and prior period accumulation. NAV per share of RM0.11 (using the 1,796m post-IPO share count as the denominator, consistent with the EPS calculation) compares to the IPO price of RM0.88, implying an IPO price-to-book of approximately 8x pre-IPO equity. Post-IPO, with RM352m of gross proceeds less approximately RM14.3m in listing expenses added to equity, the post-IPO book value would be approximately RM533.4m, implying a post-IPO price-to-book of approximately 3.0x at the IPO price, which we view as undemanding.

Figure 38: Balance Sheet Summary (FY25 vs FY26)

Balance Sheet (RM'm)	FY25	FY26	YoY Change
ASSETS			
Cash & bank balances	42.5	82.6	+94.4%
Trade & other receivables	35.2	51.6	+46.6%
Intangible assets	6.4	22.2	+247%
Plant & equipment	39.0	48.2	+23.6%
Total Assets	133.9	229.4	+71.3%
LIABILITIES & EQUITY			
Total borrowings (leases)	3.2	5.2	+62.5%
Total Equity	126.3	195.7	+55.0%
KEY METRICS			
NAV per share (RM)	0.07	0.11	+57.1%
Net cash / (debt)	39.3	77.4	+97.0%

Source: Company, Apex Securities

Key balance sheet observations. Intangible assets tripled to RM22.2m (from RM6.4m, +247% YoY), reflecting gross additions of approximately RM17.6m during FY26 representing capitalised IP development costs for next-generation products including HBM4, LPDDR6, and automotive-grade NoC IP, a leading indicator of the forward IP pipeline that should translate into future licensing revenue as these products are commercialised. Trade and other receivables grew 46.6% to RM51.6m, outpacing revenue growth of 29.7% and reflecting the Q4 revenue concentration rather than any deterioration in collection quality. Receivables days of

approximately 121 days is consistent with the milestone-based payment structure of IP licensing contracts, while customer concentration improved with 2 customers contributing RM47.4m at 10%+ of revenue in FY26, down from 3 customers contributing RM72.2m in FY25. Contract assets increased to RM7.1m (from RM0.5m in FY25), reflecting an acceleration in project execution activity ahead of billing milestones that will convert to cash receipts in the near term. Post-IPO, the Group will hold approximately RM434m in gross cash (RM82.6m existing plus RM352m IPO proceeds) with effectively zero financial debt, a net cash position of approximately RM429m representing 2.2x pre-IPO equity, providing full financial flexibility for the 36-month R&D and expansion programme without any requirement for additional financing.

Cashflow and Dividends

Operating cash flow. FY26 operating cash flow of RM61.0m was the strongest on record, driven by: (i) higher PBT of RM50.0m; (ii) non-cash add-backs including RM11.1m in depreciation and amortisation and RM1.8m in unrealised FX losses; and (iii) a broadly neutral working capital movement, with a RM16.7m increase in trade and other receivables largely offset by a RM21.5m increase in payables and a RM1.4m increase in contract liabilities. The operating cash conversion ratio (OCF/PAT) of 1.26x in FY26 represents a significant improvement from 0.66x in FY25, indicating strong and improving earnings quality - FY26 cash generation materially exceeded reported profit, confirming that earnings are not merely accounting constructs but are translating into real cash.

Key observation on cash quality. An OCF/PAT ratio above 1.0x is the hallmark of a high-quality IP licensing business where non-cash charges (D&A on capitalised IP) add back to operating cash flow in excess of working capital consumption. SkyeChip's 1.26x ratio compares favourably to the 0.66x recorded in FY25, when working capital consumed cash disproportionately as the custom ASIC segment ramped. The recovery to above 1.0x confirms the business has reached a more mature operating cadence where cash generation reliably tracks and exceeds reported earnings.

Capital expenditure. Investing cash outflow of RM39.3m in FY26 was driven by: (i) RM17.8m in plant and equipment additions, primarily engineering tools for mask sets, prototypes, and computing infrastructure; (ii) approximately RM17.6m in gross intangible asset additions covering IP development and patent costs; and (iii) RM10.0m in new financial investments, partially offset by approximately RM5.0m in disposal proceeds. This capex level is consistent with the Group's growth-stage investment in next-generation IP and ASIC capabilities. Post-IPO, with RM211.5m (60.1% of gross proceeds) earmarked for R&D of IC products and silicon IP and a further RM93.8m (26.6%) for facilities, computing infrastructure, and EDA tools, capex intensity is expected to remain elevated over the 36-month deployment horizon before normalising as the next-generation portfolio reaches commercialisation.

Dividends. SkyeChip targets a payout ratio of up to 25% of PAT attributable to owners for each financial year. No dividends were declared or paid in FY26 (nor in FPE Oct 2025), consistent with the Group conserving cash ahead of its IPO and the 36-month R&D deployment programme. In FY24, the Group declared RM19.0m in dividends (56.4% payout ratio on FY24 PAT of RM33.7m), while FY25 saw RM12.4m in dividends paid (relating to prior year declarations), reflecting pre-IPO capital returns to founding shareholders that are not expected to be repeated at this scale post-listing. We do not forecast any dividend payments in FY27F-FY29F, as we expect the Group to prioritise the full deployment of its RM352m IPO proceeds into the 36-month R&D and expansion programme (RM211.5m for IC and silicon IP R&D, RM93.8m for facilities, computing infrastructure, and EDA tools), consistent with a growth-stage company reinvesting aggressively for scale during the critical portfolio-building phase across HBM4, LPDDR6, 2nm node migration, and potential Arm CSS-based products. We expect dividends to resume from FY30F onwards once the IPO-funded R&D programme is substantially complete and operating cash flow (forecast at RM125m+ by FY30F) provides ample capacity for both continued investment and shareholder returns. Assuming a gradual ramp toward the stated 25% payout target from FY30F, the implied DPS would reach 3.44 sen by FY31F on our PAT estimate of RM247.3m.

Figure 39: Cashflow Summary (FY23-26)

Cash Flow (RM'm)	FY23	FY24	FY25	FY26
Operating CF	42.6	4.8	23.7	61.0
Investing CF	(33.1)	2.9	(20.6)	(39.3)
Financing CF	(1.5)	(13.6)	15.5	19.7
Net increase / (decrease)	7.9	(5.9)	18.7	41.3
Opening cash	21.6	29.5	24.9	42.5
Closing cash	29.5	24.9	42.5	82.6

Source: Company, Apex Securities

Valuation & Recommendation

Initiating Coverage. We initiate coverage on SKYECHIP with a BUY rating and a target price of RM4.67, based on 76.6x mid-FY28F Core EPS of 6.1 sen (a 15% premium to the 66.1x peer average FY27 forward P/E). We like SKYECHIP for: (i) the scalable IP licensing flywheel driving gross margin expansion from 45.1% to 54.7% over the forecast period; (ii) exceptional FY26 results which beat prospectus guidance (Q4 GPM 64.0%, US revenue surging to 23.1% of Group); (iii) a deep post-IPO balance sheet (c.RM434m net cash) funding RM211.5m in R&D without dilution risk; and (iv) unpriced optionality from the signed AFA definitive agreement (23 June 2026), conditional CSS approval, and Samsung Foundry CONNECT listing.

At the current price of RM2.97, SKYECHIP trades at 57.2x FY27 P/E and 41.9x FY28 P/E, a 14% and 5% discount to peer averages of 66.1x and 44.2x respectively, despite a FY26-29F core earnings CAGR of c.48% that exceeds all peers except GUC (109.8%) and Faraday (57.8%). Our 76.6x target multiple sits below Arm (162.0x) and GUC (104.1x), but above M31 (66.3x), Faraday (55.8x), and Rambus (43.4x), reflecting SkyeChip's superior growth profile and ASEAN scarcity premium while acknowledging China concentration (62.6% of FY26 revenue), Pioneer Status renewal uncertainty, and the early-stage listed track record.

Figure 40: Peer average

Stock	Mkt Cap (RM m)	Price (local)	Target	FYE	EPS		EPS Growth 27-28	P/E (x)		P/B (x)		Yield (%)	
					FY27F	FY28F		FY27	FY28	FY27	FY28	FY27	FY28
SkyeChip	5334	2.97	4.67	03/2027	0.05	0.07	36.6%	57.2	41.9	9.9	8.7	0.3%	13.7%
Oppstar	394	0.61	NR	03/2027	0.01	0.02	66.7%	50.8	30.5	3.1	2.8	0.0%	0.0%
Arm Holdings	1525003	356.95	NR	03/2027	2.20	3.04	38.0%	162.0	117.4	36.2	27.7	0.0%	0.0%
Rambus	55509	128.33	NR	12/2026	2.96	3.66	23.8%	43.4	35.1	8.4	6.9	0.0%	0.0%
Synopsys	357009	466.12	NR	10/2026	14.79	17.22	16.5%	31.5	27.1	2.7	2.7	0.0%	0.0%
Cadence	415390	376.51	NR	12/2026	7.96	9.38	17.8%	47.3	40.1	14.7	12.5	0.0%	0.0%
Global Unichip	86050	4880.00	NR	12/2026	46.86	98.32	109.8%	104.1	49.6	39.4	18.7	0.5%	0.7%
Faraday Technology	7902	230.50	NR	12/2026	4.13	6.52	57.8%	55.8	35.4	4.4	4.0	1.1%	1.8%
M31 Technology	2775	501.00	NR	12/2026	7.56	12.47	65.0%	66.3	40.2	9.6	8.3	0.7%	1.8%
Socionext	12232	2650.50	NR	03/2027	79.58	118.58	49.0%	33.3	22.4	3.4	3.2	2.0%	2.1%
Simple Average								66.1	44.2	13.5	9.6	0.5%	0.7%

Source: Apex Securities, Bloomberg

Financial Highlights

Income Statement

FYE Mar (RM m)	FY25	FY26	FY27F	FY28F	FY29F
Revenue	119.5	155.0	212.9	276.0	344.9
Gross Profit	50.4	69.9	103.5	138.1	175.7
EBITDA	43.4	60.5	107.7	150.1	196.4
EBIT	36.5	49.2	87.6	119.7	153.7
Depreciation & Amortisation	6.9	11.1	21.2	32.6	45.3
Net Finance Income/(Cost)	0.5	0.8	6.4	9.7	7.7
Associates & JV	-	-	-	-	-
Other Income/(Cost)	(0.0)	0.0	-	-	-
Pre-tax Profit	37.0	50.0	94.0	129.4	161.4
Tax	(1.1)	(1.5)	(3.8)	(5.8)	(6.5)
Profit After Tax	35.9	48.5	90.2	123.6	154.9
Minority Interest	-	-	-	-	-
Net Profit	36.0	48.2	90.2	123.6	154.9
Exceptionals	1.2	1.5	3.0	3.8	4.7
Core Net Profit	37.1	49.7	93.2	127.4	159.6

Key Ratios

FYE Mar (RM m)	FY25	FY26	FY27F	FY28F	FY29F
EPS (sen)	2.1	2.8	5.2	7.1	8.9
P/E (x)	146.1	109.1	58.2	42.6	34.0
P/B (x)	42.9	27.7	8.7	7.3	6.0
EV/EBITDA (x)	124.2	88.4	46.3	32.7	24.4
DPS (sen)	0.0	0.0	0.0	0.0	0.0
Dividend Yield (%)	-	-	-	-	-
EBITDA margin (%)	36.3%	39.0%	50.6%	54.4%	57.0%
EBIT margin (%)	30.6%	31.7%	41.2%	43.4%	44.6%
PBT margin (%)	31.0%	32.3%	44.2%	46.9%	46.8%
PAT margin (%)	30.1%	31.3%	42.4%	44.8%	44.9%
NP margin (%)	30.1%	31.1%	42.4%	44.8%	44.9%
CNP margin (%)	31.1%	32.1%	43.8%	46.1%	46.3%
ROE (%)	29.4%	25.3%	14.9%	17.0%	17.8%
ROA (%)	27.7%	21.7%	14.1%	16.0%	16.6%
Gearing (%)	2.5%	2.7%	1.0%	1.2%	1.5%
Net gearing (%)	NET CASH	NET CASH	NET CASH	NET CASH	NET CASH

Valuations

	Mid - FY28F
Core EPS (sen)	6.1
P/E Multiple (x)	76.0
Fair Value (RM)	4.67
ESG premium/discount	-
Implied Fair Value (RM)	4.67

Balance Sheet

FYE Mar (RM m)	FY25	FY26	FY27F	FY28F	FY29F
Cash	42.5	82.6	441.3	525.1	637.6
Receivables	35.2	50.6	62.7	80.8	98.4
Inventories	-	-	-	-	-
Other current assets	7.9	19.7	44.3	41.6	40.9
Total Current Assets	85.5	152.9	548.3	647.4	776.8
Fixed Assets	39.0	48.2	72.6	98.4	122.1
Intangibles	6.4	22.2	31.2	40.1	47.3
Other non-current assets	3.0	6.1	7.9	10.8	15.8
Total Non-Current Assets	48.4	76.5	111.7	149.3	185.2
Short-term debt	1.2	1.4	2.5	3.0	3.7
Payables	2.7	24.2	22.8	28.3	34.3
Other current liabilities	0.1	2.1	3.1	4.3	4.7
Total Current Liabilities	4.0	27.7	28.4	35.6	42.7
Long-term debt	2.0	3.8	3.9	6.0	10.1
Other non-current liabilities	1.6	2.2	4.2	8.3	12.9
Total Non-Current Liabilities	3.6	5.9	8.1	14.3	23.1
Shareholder's equity	126.3	195.7	623.5	746.7	896.3
Minority interest	-	-	-	-	-
Total Equity	126.3	195.7	623.5	746.7	896.3

Cash Flow

FYE Mar (RM m)	FY25	FY26	FY27F	FY28F	FY29F
Pre-tax profit	37.0	50.0	94.0	129.4	161.4
Depreciation & amortisation	6.9	11.1	21.2	32.6	45.3
Changes in working capital	(20.1)	(0.4)	(15.7)	(14.5)	(13.4)
Others	(0.1)	0.2	(8.0)	(11.8)	(10.2)
Operating cash flow	23.7	61.0	91.5	135.7	183.1
Net capex	(36.8)	(35.4)	(53.5)	(65.1)	(73.6)
Others	16.2	(3.9)	(15.3)	16.0	11.4
Investing cash flow	(20.6)	(39.3)	(68.8)	(49.1)	(62.2)
Dividends paid	(12.4)	-	-	-	(5.0)
Others	27.9	19.7	336.2	(2.5)	(3.0)
Financing cash flow	15.5	19.7	336.2	(2.5)	(8.0)
Net cash flow	18.7	41.3	358.9	84.1	112.9
Forex	(1.1)	(1.2)	(0.2)	(0.3)	(0.4)
Others	-	-	-	-	-
Beginning cash	24.9	42.5	82.6	441.3	525.1
Ending cash	42.5	82.6	441.3	525.1	637.6

Source: Company, Apex Securities

ESG Matrix Framework:

Environment

Parameters	Rating	Comments
Climate	★★★	Qualitative commitment to national 2050 net-zero aspiration
Waste & Effluent	★★★	Fabless model limits waste streams to office and e-waste
Energy	★★★	Energy-saving initiatives limited to LED lighting and automatic AC scheduling
Water	★★★	Usage limited to drinking water and sanitary facilities
Compliance	★★★	No environmental non-compliance incidents reported, no ISO 14001 certification held

Social

Diversity	★★★	26.1% of employees are female, 98.7% local workforce, ~429 total employees with 365 technical staff
Human Rights	★★★	Enforces Code of Conduct and Ethics, Anti-Bribery Policy and Whistleblowing Policy aligned with MACC Act 2009
Occupational Safety and Health	★★	HSE committee holds quarterly meetings with annual fire drills
Labour Practices	★★★	New engineers complete 110 hours of training across 25 modules, average engineer cost ~USD38k/year, ESOS of up to 15% of issued shares

Governance

CSR Strategy	★★★	RM280,013 invested in sponsoring final-year IC design projects at UTM, UPM and UniMAP
Management	★★★	2/6 female board composition (33%), 4/6 Independent Directors (67%), Chairman/CEO roles separated, full MCGG adoption with no departures
Stakeholders	★★★	Newly listed (20 May 2026), no AGM held yet, IPO oversubscribed 95.03x with 22 cornerstone investors including EPF and Khazanah

Overall ESG Scoring: ★★★

Recommendation Framework:

BUY: Total returns* are expected to exceed 10% within the next 12 months.

HOLD: Total returns* are expected to be within +10% to -10% within the next 12 months.

SELL: Total returns* are expected to be below -10% within the next 12 months.

TRADING BUY: Total returns* are expected to exceed 10% within the next 3 months.

TRADING SELL: Total returns* are expected to be below -10% within the next 3 months.

*Capital gain + dividend yield

Sector Recommendations:

OVERWEIGHT: The industry defined by the analyst is expected to exceed 10% within the next 12 months.

NEUTRAL: The industry defined by the analyst is expected to be within +10% to -10% within the next 12 months.

UNDERWEIGHT: The industry defined by the analyst, is expected to be below -10% within the next 12 months.

ESG Rating Framework:

★★★★★ : Appraised with 3% premium to fundamental fair value

★★★★ : Appraised with 1% premium to fundamental fair value

★★★ : Appraised with 0% premium/discount to fundamental fair value

★★ : Appraised with -1% discount to fundamental fair value

★ : Appraised with -5% discount to fundamental fair value

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(a) nil.